

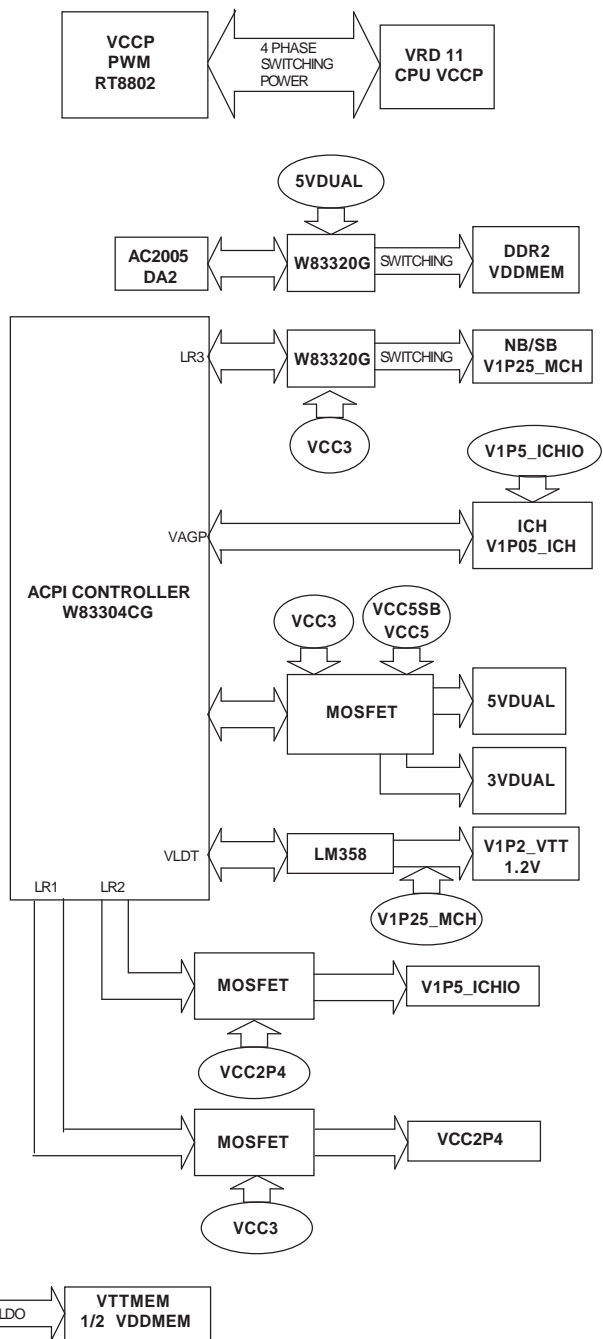
ABIT - IP35 Pro SCHEMATICS

Version: 0.2

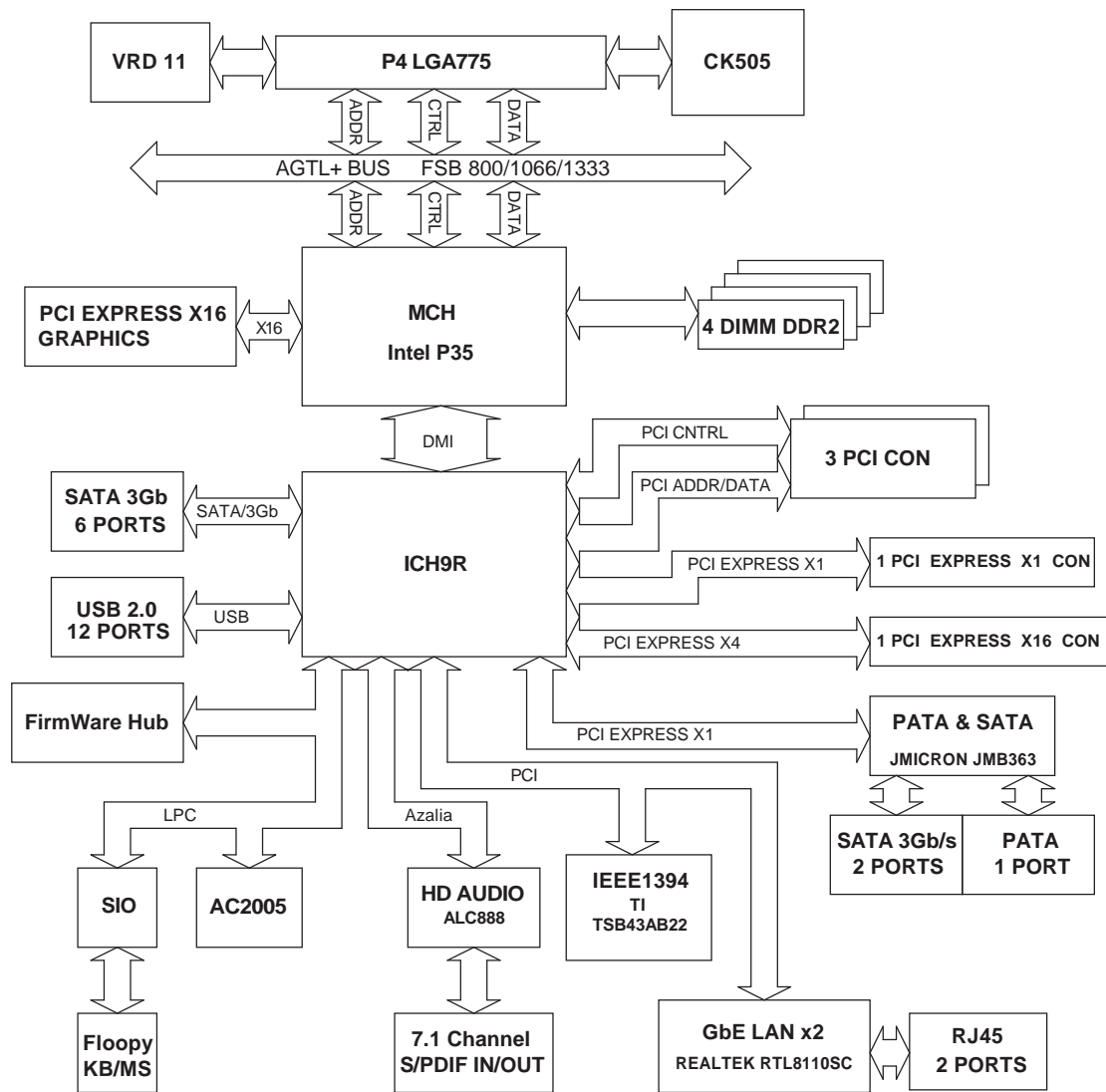
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Model	Features
IP35 Pro	uGuru Tech., Silent OTES 2, Dual DDR2 800, Dual SATA 3Gb/s RAID, eSATA, PATA, GbE, IEEE -1394, 7.1 Channel HD Audio

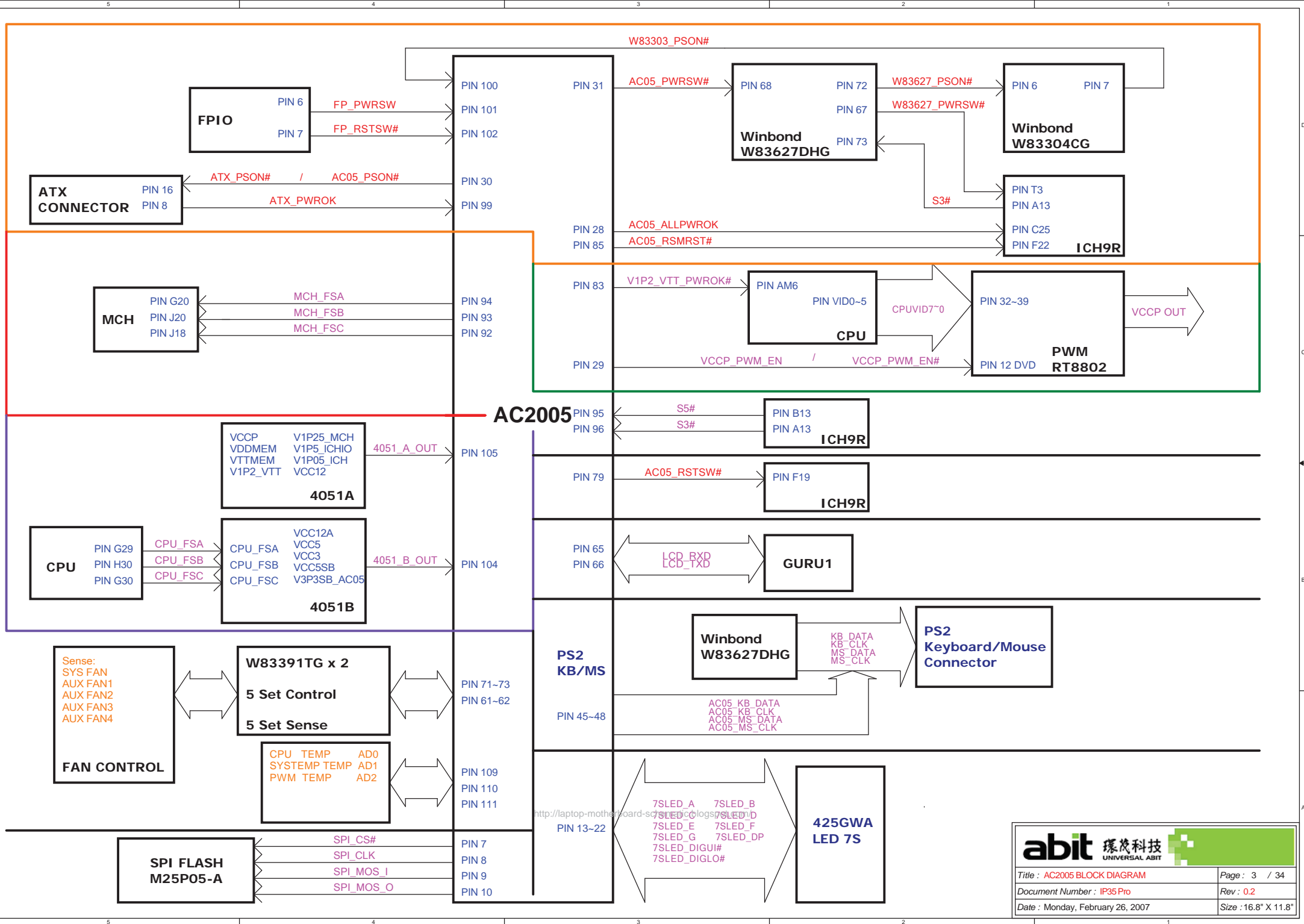
POWER DESIGN DIAGRAM



BLOCK DIAGRAM



<http://laptop-motherboard-schematic.blogspot.com/>



ICH9 GPIO SETTING

Pin Name	Power Well	Usage	Default
GPIO0	3.3V Core	ACZ_DET	GPI
GPIO1	3.3V Core	TACH1	GPI
GPIO2	5V Core	PIRQ#E	GPI
GPIO3	5V Core	PIRQ#F	GPI
GPIO4	5V Core	PIRQ#G	GPI
GPIO5	5V Core	PIRQ#H	GPI
GPIO6	3.3V Core	TACH2	GPI
GPIO7	3.3V Core	TACH3	GPI
GPIO8	3.3V Sus	LPC_PME#	GPI
GPIO9	3.3V Sus	WOL_EN	Native
GPIO10	3.3V Sus	LAN_PME2#	GPI
GPIO11	3.3V Sus	SMBALERT#	Native
GPIO12	3.3V Sus	LAN_PME#	GPI
GPIO13	3.3V Sus	1394_PME#	GPI
GPIO14	3.3V Sus	GPIO14	GPI
GPIO15	3.3V Sus	GPIO15	Native
GPIO16	3.3V Core	FWH_WP#	GPO
GPIO17	3.3V Core	TACH0	GPI
GPIO18	3.3V Core	GPIO18	GPO
GPIO19	3.3V Core	SATA1GP	GPI
GPIO20	3.3V Core	GPIO20	GPO
GPIO21	3.3V Core	SATA0GP	GPI
GPIO22	3.3V Core	SCLOCK	Native
GPIO23	3.3V Core	LDRQ1#	Native
GPIO24	3.3V Sus	CLGPIO0	GPO
GPIO25	3.3V Sus	STP_CPU#	Native
GPIO26	3.3V Sus	S4_SATE#	GPO
GPIO27	3.3V Sus	EL_STATE0	GPO
GPIO28	3.3V Sus	EL_STATE1	GPO
GPIO29	3.3V Sus	OC5#	Native
GPIO30	3.3V Sus	OC6#	Native
GPIO31	3.3V Sus	OC7#	Native
GPIO32	3.3V Core	GIPO32	GPO
GPIO33	3.3V Core	GIOP33	GPO
GPIO34	3.3V Core	BOARD ID	GPO
GPIO35	3.3V Core	BOARD ID	GPO
GPIO36	3.3V Core	SATA2GP	GPI
GPIO37	3.3V Core	SATA3GP	GPI
GPIO38	3.3V Core	SLOAD	GPI
GPIO39	3.3V Core	SDATAOUT0	GPI
GPIO40	3.3V Sus	OC1#	Native
GPIO41	3.3V Sus	OC2#	Native
GPIO42	3.3V Sus	OC3#	Native
GPIO43	3.3V Sus	OC4#	Native
GPIO44	3.3V Sus	OC8#	Native
GPIO45	3.3V Sus	OC9#	Native
GPIO46	3.3V Sus	OC10#	Native
GPIO47	3.3V Sus	OC11#	Native
GPIO48	3.3V Core	SDATAOUT0	GPI
GPIO49	V_CPU_IO	GPIO49	Native
GPIO50	5.5V Core	REQ1#	Native
GPIO51	3.3V Core	GNT1#	Native
GPIO52	5.5V Core	REQ2#	Native
GPIO53	3.3V Core	GNT2#	Native
GPIO54	5.5V Core	REQ3#	Native
GPIO55	3.3V Core	GNT3#	Native

W83304CG Voltage Adjust Table

a.CR07[3:0]

V1P25_OV	Bit3	Bit2	Bit1	Bit0	V1P25_MCH	
0/1	0	0	0	0	1.25/1.807V	0.8
0/1	0	0	0	1	1.289/1.864V	0.825
0/1	0	0	1	0	1.328/1.920V	0.850
0/1	0	0	1	1	1.367/1.977V	0.875
0/1	0	1	0	0	1.406/2.034V	0.900
0/1	0	1	0	1	1.445/2.090V	0.925
0/1	0	1	1	0	1.484/2.146V	0.950
0/1	0	1	1	1	1.523/2.203V	0.975
0/1	1	0	0	0	1.562/2.259V	1.00
0/1	1	0	0	1	1.640/2.373V	1.050
0/1	1	0	1	0	1.718/2.486V	1.100

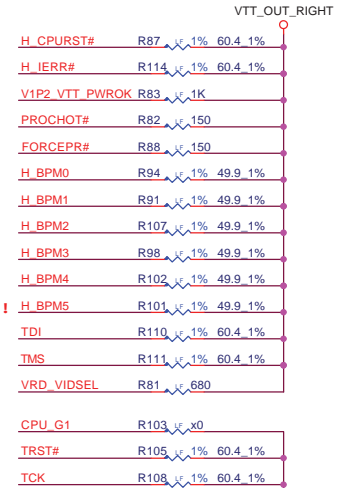
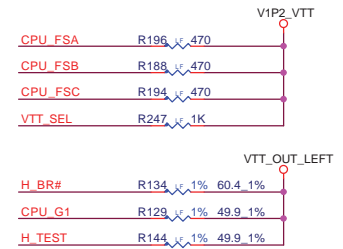
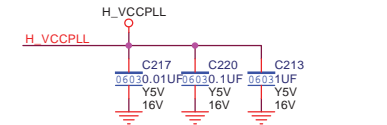
b.CR04(Over Voltage Configuration Register for VLDT,Default 0x00h, Read/write)

VTT_SEL	Bit2	Bit1	Bit0	V1P2_VTT
0/1	0	0	0	1.10V/1.20V
0/1	0	0	1	1.15V/1.25V
0/1	0	1	0	1.20V/1.30V
0/1	0	1	1	1.25V/1.35V
0/1	1	0	0	1.30V/1.40V
0/1	1	0	1	1.35V/1.45V
0/1	1	1	0	1.40V/1.50V

V1P2_VTT should be synchronized w/ V1P25_MCH

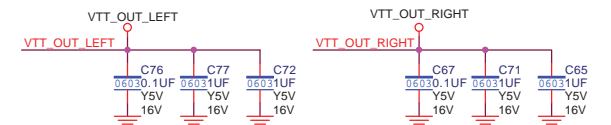
PCI DEVICE SETTING

DEVICE	PCI1	PCI2	PCI3	1394	GbE1	GbE2
INTA	G	H	E	F	G	H
INTB	H	E	F	G	H	E
INTC	E	F	G			
INTD	F	G	H			
IDSEL	19	20	21	18	17	16
REQ/GNT	3A	3B	3C	2	1	0



MSID0	MSID1	Description
0	0	Intel Core 2 Duo
0	1	Reserved
1	0	Reserved
1	1	Intel Core 2 Quad

KENTSFIELD SUPPORT





U12C U1MCH

M MAA_A0	BB30	DDR_A_MA_0	AP2	M DQS_P_A0
M MAA_A1	AY25	DDR_A_MA_1	AP3	M DQS_N_A0
M MAA_A2	BA23	DDR_A_DM_0	AN2	M DQM_A0
M MAA_A3	BB23	DDR_A_MA_2		
M MAA_A4	AY23	DDR_A_MA_3	AM1	M DATA_A0
M MAA_A5	BB22	DDR_A_MA_4	AN3	M DATA_A1
M MAA_A6	BA22	DDR_A_MA_5	AR2	M DATA_A2
M MAA_A7	BB21	DDR_A_MA_6	AR3	M DATA_A3
M MAA_A8	AW21	DDR_A_MA_7	AL3	M DATA_A4
M MAA_A9	BA21	DDR_A_MA_8	AM2	M DATA_A5
M MAA_A10	BB31	DDR_A_MA_9	AR5	M DATA_A6
M MAA_A11	AY21	DDR_A_MA_10	AR4	M DATA_A7
M MAA_A12	BC20	DDR_A_MA_11		
M MAA_A13	AY38	DDR_A_MA_12	AW2	M DQS_P_A1
M MAA_A14	BA19	DDR_A_MA_13	AW1	M DQS_N_A1
		DDR_A_MA_14	AW3	M DQM_A1

11,13 M_WE_A	BA33	DDR_A_WEB
11,13 M_CAS_A	AW35	DDR_A_CASB
11,13 M_RAS_A	AY33	DDR_A_RASB

11,13 M_SBA_A0	BA31	DDR_A_BS_0
11,13 M_SBA_A1	AY31	DDR_A_BS_1
11,13 M_SBA_A2	AY20	DDR_A_BS_2

11,13 M_SCS_A0	BA34	DDR_A_CSB_0
11,13 M_SCS_A1	AY35	DDR_A_CSB_1
11,13 M_SCS_A2	BB33	DDR_A_CSB_2
11,13 M_SCS_A3	BB38	DDR_A_CSB_3

11,13 M_SCKE_A0	AY19	DDR_A_CKE_0
11,13 M_SCKE_A1	AW18	DDR_A_CKE_1
11,13 M_SCKE_A2	BB19	DDR_A_CKE_2
11,13 M_SCKE_A3	BA18	DDR_A_CKE_3

11,13 M_SODT_A0	BB35	DDR_A_ODT_0
11,13 M_SODT_A1	BA38	DDR_A_ODT_1
11,13 M_SODT_A2	BA35	DDR_A_ODT_2
11,13 M_SODT_A3	BA39	DDR_A_ODT_3

11 CK_M_DDR_P_A0	AR31	DDR_A_CK_0
11 CK_M_DDR_N_A0	AU31	DDR_A_CKB_0
11 CK_M_DDR_P_A1	AP27	DDR_A_CK_1
11 CK_M_DDR_N_A1	AN27	DDR_A_CKB_1
11 CK_M_DDR_P_A2	AV33	DDR_A_CK_2
11 CK_M_DDR_N_A2	AW33	DDR_A_CKB_2
11 CK_M_DDR_P_A3	AP29	DDR_A_CK_3
11 CK_M_DDR_N_A3	AP31	DDR_A_CKB_3
11 CK_M_DDR_P_A4	AM26	DDR_A_CK_4
11 CK_M_DDR_N_A4	AM27	DDR_A_CKB_4
11 CK_M_DDR_P_A5	AT33	DDR_A_CK_5
11 CK_M_DDR_N_A5	AU33	DDR_A_CKB_5

DDR_A_MA_0	AP2	M DQS_P_A0
DDR_A_MA_1	AP3	M DQS_N_A0
DDR_A_MA_2	AN2	M DQM_A0
DDR_A_MA_3		
DDR_A_MA_4	AM1	M DATA_A0
DDR_A_MA_5	AN3	M DATA_A1
DDR_A_MA_6	AR2	M DATA_A2
DDR_A_MA_7	AR3	M DATA_A3
DDR_A_MA_8	AL3	M DATA_A4
DDR_A_MA_9	AM2	M DATA_A5
DDR_A_MA_10	AR5	M DATA_A6
DDR_A_MA_11	AR4	M DATA_A7

DDR_A_DQS_1	AW2	M DQS_P_A1
DDR_A_DQS_2	AW1	M DQS_N_A1
DDR_A_DQS_3	AW3	M DQM_A1
DDR_A_DM_1		

DDR_A_WEB	AV4	M DATA_A8
DDR_A_CASB	AV3	M DATA_A9
DDR_A_RASB	BA4	M DATA_A10
DDR_A_BS_0	BB3	M DATA_A11
DDR_A_BS_1	AU2	M DATA_A12
DDR_A_BS_2	AU1	M DATA_A13
DDR_A_BS_3	AY2	M DATA_A14
DDR_A_BS_4	AY3	M DATA_A15

DDR_A_CSB_0	AY7	M DQS_P_A2
DDR_A_CSB_1	BA6	M DQS_N_A2
DDR_A_CSB_2	BB6	M DQM_A2
DDR_A_CSB_3		

DDR_A_CKE_0	BB5	M DATA_A16
DDR_A_CKE_1	AY6	M DATA_A17
DDR_A_CKE_2	BA9	M DATA_A18
DDR_A_CKE_3	BB9	M DATA_A19
DDR_A_CKE_4	BA5	M DATA_A20
DDR_A_CKE_5	BB4	M DATA_A21
DDR_A_CKE_6	BC7	M DATA_A22
DDR_A_CKE_7	AY9	M DATA_A23

DDR_A_DQS_3	AT20	M DQS_P_A3
DDR_A_DQS_4	AU18	M DQS_N_A3
DDR_A_DQS_5	AN18	M DQM_A3
DDR_A_DM_3		
DDR_A_MA_24	AT18	M DATA_A24
DDR_A_MA_25	AR18	M DATA_A25
DDR_A_MA_26	AU21	M DATA_A26
DDR_A_MA_27	AT21	M DATA_A27
DDR_A_MA_28	AP17	M DATA_A28
DDR_A_MA_29	AN17	M DATA_A29
DDR_A_MA_30	AP20	M DATA_A30
DDR_A_MA_31	AV20	M DATA_A31

DDR_A_DQS_4	AR41	M DQS_P_A4
DDR_A_DQS_5	AR40	M DQS_N_A4
DDR_A_DM_4	AU43	M DQM_A4
DDR_A_DM_4		

DDR_A_DQ_32	AV42	M DATA_A32
DDR_A_DQ_33	AU40	M DATA_A33
DDR_A_DQ_34	AP42	M DATA_A34
DDR_A_DQ_35	AN39	M DATA_A35
DDR_A_DQ_36	AV40	M DATA_A36
DDR_A_DQ_37	AV41	M DATA_A37
DDR_A_DQ_38	AR42	M DATA_A38
DDR_A_DQ_39	AP41	M DATA_A39

DDR_A_DQS_5	AL41	M DQS_P_A5
DDR_A_DQS_6	AL40	M DQS_N_A5
DDR_A_DM_5	AM43	M DQM_A5
DDR_A_DM_5		

DDR_A_DQ_40	AN41	M DATA_A40
DDR_A_DQ_41	AM39	M DATA_A41
DDR_A_DQ_42	AK42	M DATA_A42
DDR_A_DQ_43	AK43	M DATA_A43
DDR_A_DQ_44	AN40	M DATA_A44
DDR_A_DQ_45	AN42	M DATA_A45
DDR_A_DQ_46	AL42	M DATA_A46
DDR_A_DQ_47	AL39	M DATA_A47

DDR_A_DQS_6	AG42	M DQS_P_A6
DDR_A_DQS_7	AG41	M DQS_N_A6
DDR_A_DM_6	AG40	M DQM_A6
DDR_A_DM_6		

DDR_A_DQ_48	AJ40	M DATA_A48
DDR_A_DQ_49	AH43	M DATA_A49
DDR_A_DQ_50	AF39	M DATA_A50
DDR_A_DQ_51	AE40	M DATA_A51
DDR_A_DQ_52	AJ42	M DATA_A52
DDR_A_DQ_53	AJ41	M DATA_A53
DDR_A_DQ_54	AE41	M DATA_A54
DDR_A_DQ_55	AF42	M DATA_A55

DDR_A_DQS_7	AC42	M DQS_P_A7
DDR_A_DQS_8	AC41	M DQS_N_A7
DDR_A_DM_7	AC40	M DQM_A7
DDR_A_DM_7		

DDR_A_DQ_56	AD40	M DATA_A56
DDR_A_DQ_57	AD43	M DATA_A57
DDR_A_DQ_58	AB41	M DATA_A58
DDR_A_DQ_59	AA40	M DATA_A59
DDR_A_DQ_60	AE42	M DATA_A60
DDR_A_DQ_61	AE41	M DATA_A61
DDR_A_DQ_62	AC39	M DATA_A62
DDR_A_DQ_63	AB42	M DATA_A63

DDR_A

AN21 XRESERVED_1

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BRLK_B_CRB_0

U12D U1MCH

M MAA_B0	AW15	DDR_B_MA_0	AV6	M DQS_P_B0
M MAA_B1	BB15	DDR_B_MA_1	AU5	M DQS_N_B0
M MAA_B2	BA15	DDR_B_DM_0	AR7	M DQM_B0
M MAA_B3	AY15	DDR_B_MA_2		
M MAA_B4	BA14	DDR_B_MA_3	AN7	M DATA_B0
M MAA_B5	BB14	DDR_B_MA_4	AN8	M DATA_B1
M MAA_B6	AW12	DDR_B_MA_5	AW5	M DATA_B2
M MAA_B7	BB13	DDR_B_MA_6	AW7	M DATA_B3
M MAA_B8	BB13	DDR_B_MA_7	AN5	M DATA_B4
M MAA_B9	AY13	DDR_B_MA_8	AN6	M DATA_B5
M MAA_B10	BA17	DDR_B_MA_9	AN9	M DATA_B6
M MAA_B11	AY12	DDR_B_MA_10	AU7	M DATA_B7
M MAA_B12	BA11	DDR_B_MA_11		
M MAA_B13	BB11	DDR_B_MA_12	AR12	M DQS_P_B1
M MAA_B14	BB11	DDR_B_MA_13	AR15	M DQS_N_B1
		DDR_B_MA_14	AW9	M DQM_B1

12,13 M_WE_B	BB25	DDR_B_WEB
12,13 M_CAS_B	AW26	DDR_B_CASB
12,13 M_RAS_B	AY24	DDR_B_RASB

12,13 M_SBA_B0	BB17	DDR_B_BS_0
12,13 M_SBA_B1	AY17	DDR_B_BS_1
12,13 M_SBA_B2	AY11	DDR_B_BS_2

12,13 M_SCS_B0	BA25	DDR_B_CSB_0
12,13 M_SCS_B1	BA29	DDR_B_CSB_1
12,13 M_SCS_B2	BA26	DDR_B_CSB_2
12,13 M_SCS_B3	BA30	DDR_B_CSB_3

12,13 M_SCKE_B0	AW11	DDR_B_CKE_0
12,13 M_SCKE_B1	BC12	DDR_B_CKE_1
12,13 M_SCKE_B2	BA10	DDR_B_CKE_2
12,13 M_SCKE_B3	BB10	DDR_B_CKE_3

12,13 M_SODT_B0	BB27	DDR_B_ODT_0
12,13 M_SODT_B1	AW29	DDR_B_ODT_1
12,13 M_SODT_B2	BA27	DDR_B_ODT_2
12,13 M_SODT_B3	AY29	DDR_B_ODT_3

12 CK_M_DDR_P_B0	AW31	DDR_B_CK_0
12 CK_M_DDR_N_B0	AV31	DDR_B_CKB_0
12 CK_M_DDR_P_B1	AU27	DDR_B_CK_1
12 CK_M_DDR_N_B1	AT27	DDR_B_CKB_1
12 CK_M_DDR_P_B2	AT32	DDR_B_CK_2
12 CK_M_DDR_N_B2	AR28	DDR_B_CKB_2
12 CK_M_DDR_P_B3	AU29	DDR_B_CK_3
12 CK_M_DDR_N_B3	AU29	DDR_B_CKB_3
12 CK_M_DDR_P_B4	AV29	DDR_B_CK_4
12 CK_M_DDR_N_B4	AW27	DDR_B_CKB_4
12 CK_M_DDR_P_B5	AN33	DDR_B_CK_5
12 CK_M_DDR_N_B5	AF32	DDR_B_CKB_5

DDR_B_DQS_4	AW39	M DQS_P_B4
DDR_B_DQS_5	AU39	M DQS_N_B4
DDR_B_DM_4	AU37	M DQM_B4
DDR_B_DM_4		

DDR_B_DQ_32	AV37	M DATA_B32
DDR_B_DQ_33	AV38	M DATA_B33
DDR_B_DQ_34	AN36	M DATA_B34
DDR_B_DQ_35	AN37	M DATA_B35
DDR_B_DQ_36	AU35	M DATA_B36
DDR_B_DQ_37	AR35	M DATA_B37
DDR_B_DQ_38	AN35	M DATA_B38
DDR_B_DQ_39	AR37	M DATA_B39

DDR_B_DQS_5	AL35	M DQS_P_B5
DDR_B_DQS_6	AL34	M DQS_N_B5
DDR_B_DM_5	AM37	M DQM_B5
DDR_B_DM_5		

DDR_B_DQ_40	AM35	M DATA_B40
DDR_B_DQ_41	AM38	M DATA_B41
DDR_B_DQ_42	AJ34	M DATA_B42
DDR_B_DQ_43	AL38	M DATA_B43
DDR_B_DQ_44	AR39	M DATA_B44
DDR_B_DQ_45	AM34	M DATA_B45
DDR_B_DQ_46	AL37	M DATA_B46
DDR_B_DQ_47	AL32	M DATA_B47

DDR_B_DQS_6	AG35	M DQS_P_B6
DDR_B_DQS_7	AG36	M DQS_N_B6
DDR_B_DM_6	AG39	M DQM_B6
DDR_B_DM_6		

DDR_B

SVREF AM21 XRESERVED_10

DDR_VREF AM6

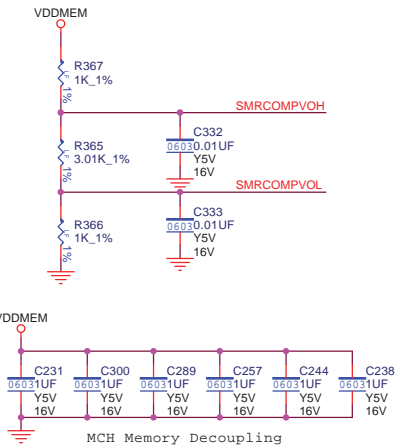
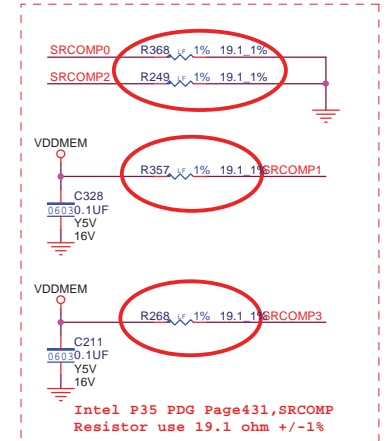
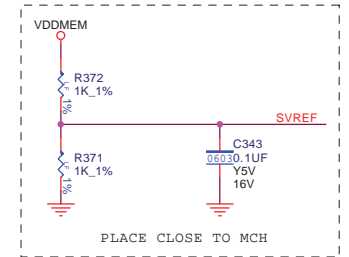
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SRCOMP0	AL4
SRCOMP1	AL2
SRCOMP2	BB40
SRCOMP3	BA40
SMRCOMPVOL	AM8
SMRCOMPVOH	AM10

DDR_B_DQ_56	AD36	M DATA_B56
DDR_B_DQ_57	AC33	M DATA_B57
DDR_B_DQ_58	AA34	M DATA_B58
DDR_B_DQ_59	AD34	M DATA_B59
DDR_B_DQ_60	AE38	M DATA_B60
DDR_B_DQ_61	AC34	M DATA_B61
DDR_B_DQ_62	AA33	M DATA_B62
DDR_B_DQ_63		

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BRLK_B_CRB_0



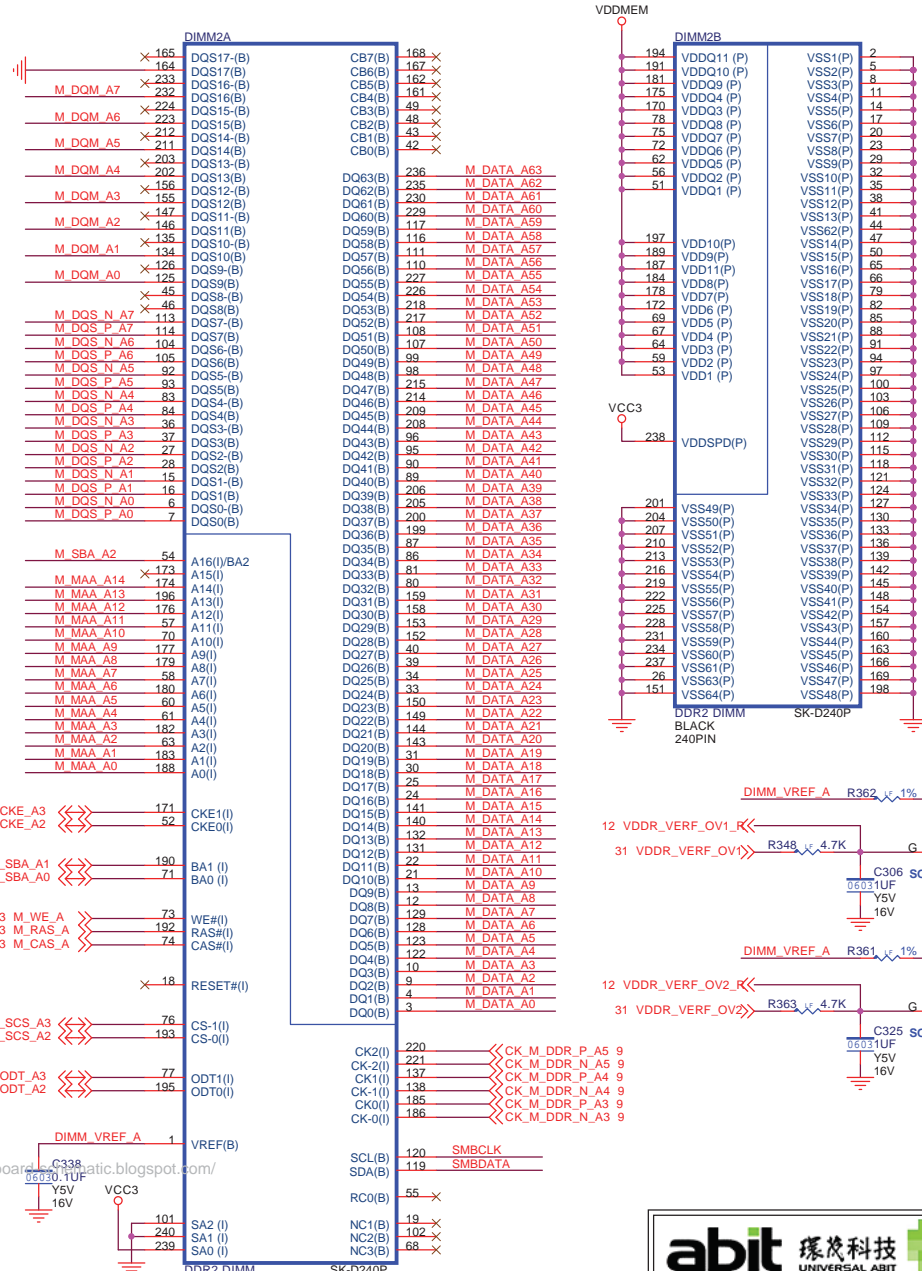
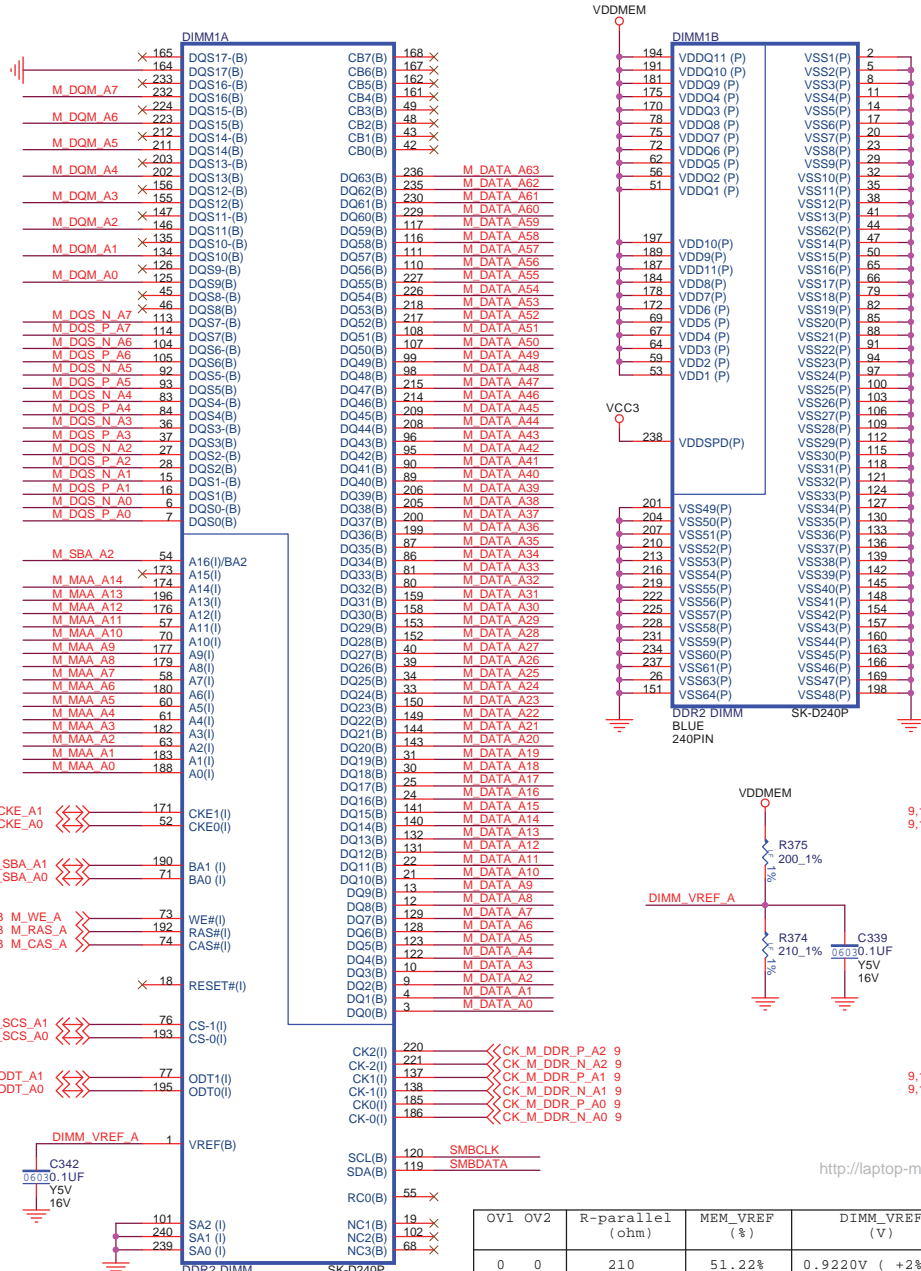
M_DQM_A[0..7] <=> M_DQM_A[0..7] 9
M_DATA_A[0..63] <=> M_DATA_A[0..63] 9

M_MAA_A[0..14] <=> M_MAA_A[0..14] 9,13
M_DQS_P_A[0..7] <=> M_DQS_P_A[0..7] 9
M_DQS_N_A[0..7] <=> M_DQS_N_A[0..7] 9




M_SBA_A2 <=> M_SBA_A2 9,13
SMBDATA <=> SMBDATA 12,14,16,18,23,26
SMBCLK <=> SMBCLK 12,14,16,18,23,26

Channel A DIMM1

Channel A DIMM2



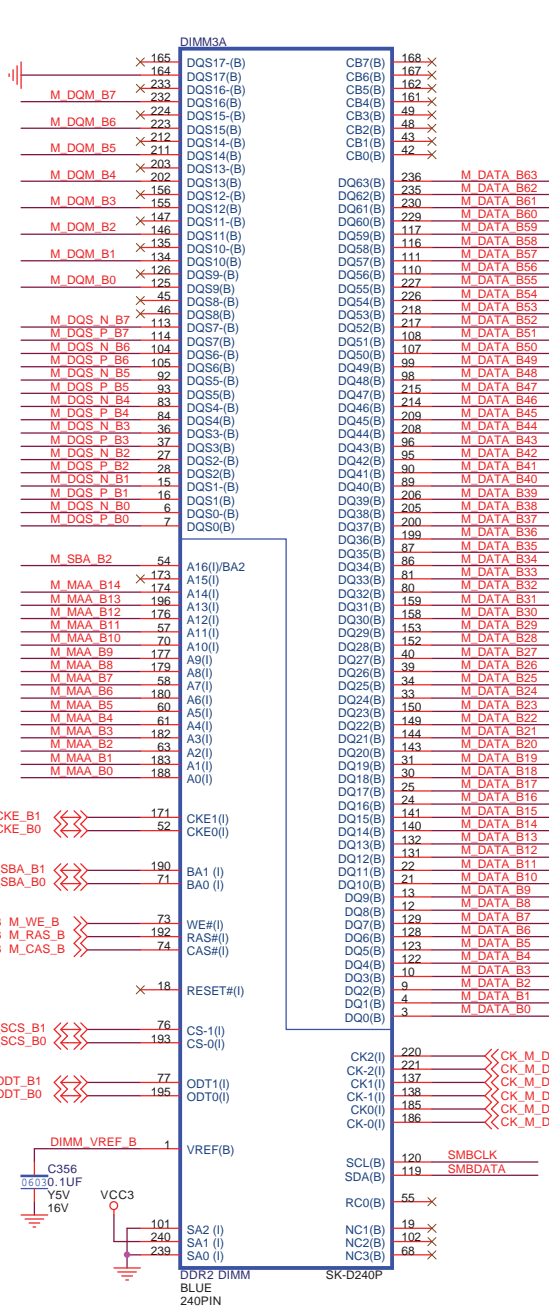
OV1	OV2	R-parallel (ohm)	MEM_VREF (%)	DIMM_VREF (V)
0	0	210	51.22%	0.9220V (+2%)
0	1	192.145	49.0%	0.8820V (-2%)
1	0	199.574	49.95%	0.8991V (default)
1	1	183.381	47.83%	0.8609V (-4%)



Title : DDR2 CHANNEL A	Page : 11 / 34
Document Number : IP35Pro	Rev : 0.2
Date : Monday, February 26, 2007	Size : 16.8" X 11.8"

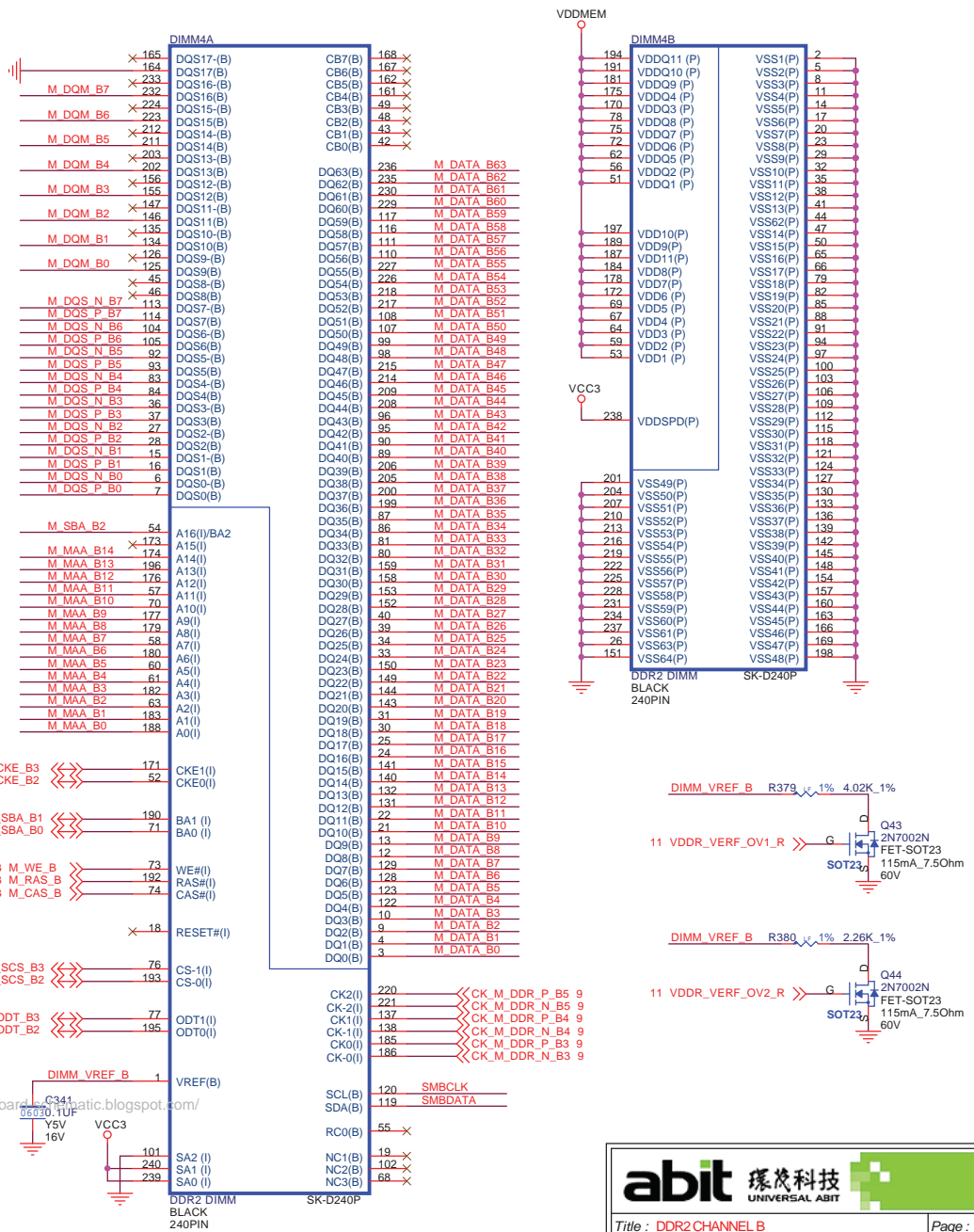


Channel B DIMM1



ADDRESS=010

Channel B DIMM2



ADDRESS=011

9,11 M_MAA_A[0..14] >> M_MAA_A[0..14]

9,12 M_MAA_B[0..14] >> M_MAA_B[0..14]

M_MAA_A0 R182 33 0402
M_MAA_A1 R204 33 0402
M_MAA_A2 R206 33 0402
M_MAA_A3 R210 33 0402
M_MAA_A4 R213 33 0402
M_MAA_A5 R218 33 0402
M_MAA_A6 R216 33 0402
M_MAA_A7 R225 33 0402
M_MAA_A8 R220 33 0402
M_MAA_A9 R228 33 0402
M_MAA_A10 R183 33 0402
M_MAA_A11 R230 33 0402
M_MAA_A12 R234 33 0402
M_MAA_A13 R161 33 0402
M_MAA_A14 R245 33 0402

9,11 M_SBA_A0 >> R180 33 0402
9,11 M_SBA_A1 >> R187 33 0402
9,11 M_SBA_A2 >> R240 33 0402
9,11 M_WE_A >> R173 33 0402
9,11 M_RAS_A >> R175 33 0402
9,11 M_CAS_A >> R160 33 0402

9,11 M_SODT_A0 >> R165 43 0402
9,11 M_SODT_A1 >> R157 43 0402
9,11 M_SODT_A2 >> R167 43 0402
9,11 M_SODT_A3 >> R155 43 0402

9,11 M_SCKE_A0 >> R257 43 0402
9,11 M_SCKE_A1 >> R267 43 0402
9,11 M_SCKE_A2 >> R250 43 0402
9,11 M_SCKE_A3 >> R270 43 0402

9,11 M_SCS_A0 >> R169 43 0402
9,11 M_SCS_A1 >> R162 43 0402
9,11 M_SCS_A2 >> R171 43 0402
9,11 M_SCS_A3 >> R159 43 0402

M_MAA_B0 R198 33 0402
M_MAA_B1 R212 33 0402
M_MAA_B2 R209 33 0402
M_MAA_B3 R215 33 0402
M_MAA_B4 R217 33 0402
M_MAA_B5 R219 33 0402
M_MAA_B6 R223 33 0402
M_MAA_B7 R229 33 0402
M_MAA_B8 R227 33 0402
M_MAA_B9 R232 33 0402
M_MAA_B10 R193 33 0402
M_MAA_B11 R235 33 0402
M_MAA_B12 R239 33 0402
M_MAA_B13 R172 33 0402
M_MAA_B14 R244 33 0402

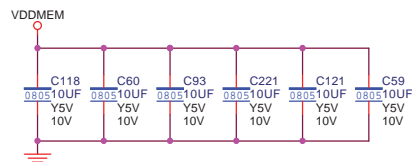
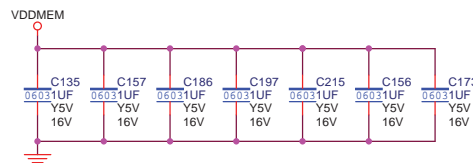
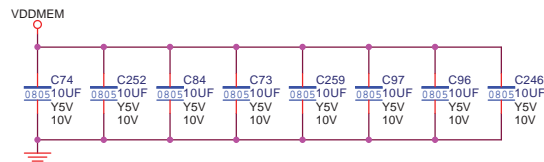
9,12 M_SBA_B0 >> R191 33 0402
9,12 M_SBA_B1 >> R195 33 0402
9,12 M_SBA_B2 >> R248 33 0402

9,12 M_WE_B >> R185 33 0402
9,12 M_RAS_B >> R189 33 0402
9,12 M_CAS_B >> R176 33 0402

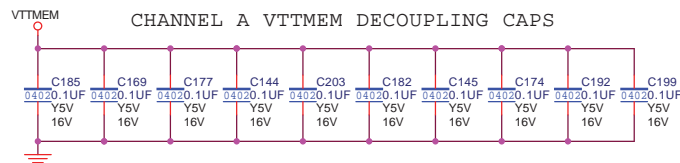
9,12 M_SODT_B0 >> R158 43 0402
9,12 M_SODT_B1 >> R156 43 0402
9,12 M_SODT_B2 >> R174 43 0402
9,12 M_SODT_B3 >> R166 43 0402

9,12 M_SCKE_B0 >> R252 43 0402
9,12 M_SCKE_B1 >> R273 43 0402
9,12 M_SCKE_B2 >> R268 43 0402
9,12 M_SCKE_B3 >> R266 43 0402

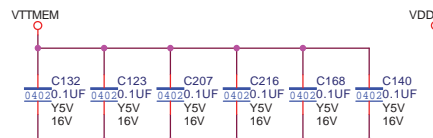
9,12 M_SCS_B0 >> R170 43 0402
9,12 M_SCS_B1 >> R168 43 0402
9,12 M_SCS_B2 >> R181 43 0402
9,12 M_SCS_B3 >> R163 43 0402



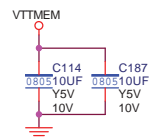
Place Near DIMM



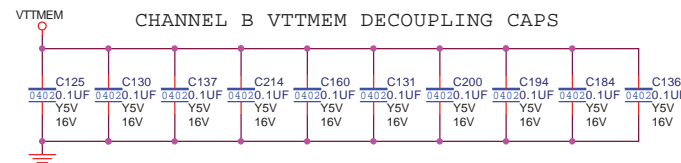
CHANNEL A VTTMEM DECOUPLING CAPS



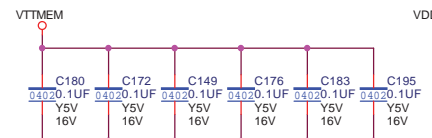
Channel A Address/Control switching Caps



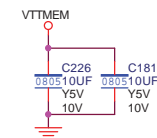
place at left and right ends of VTT island



CHANNEL B VTTMEM DECOUPLING CAPS



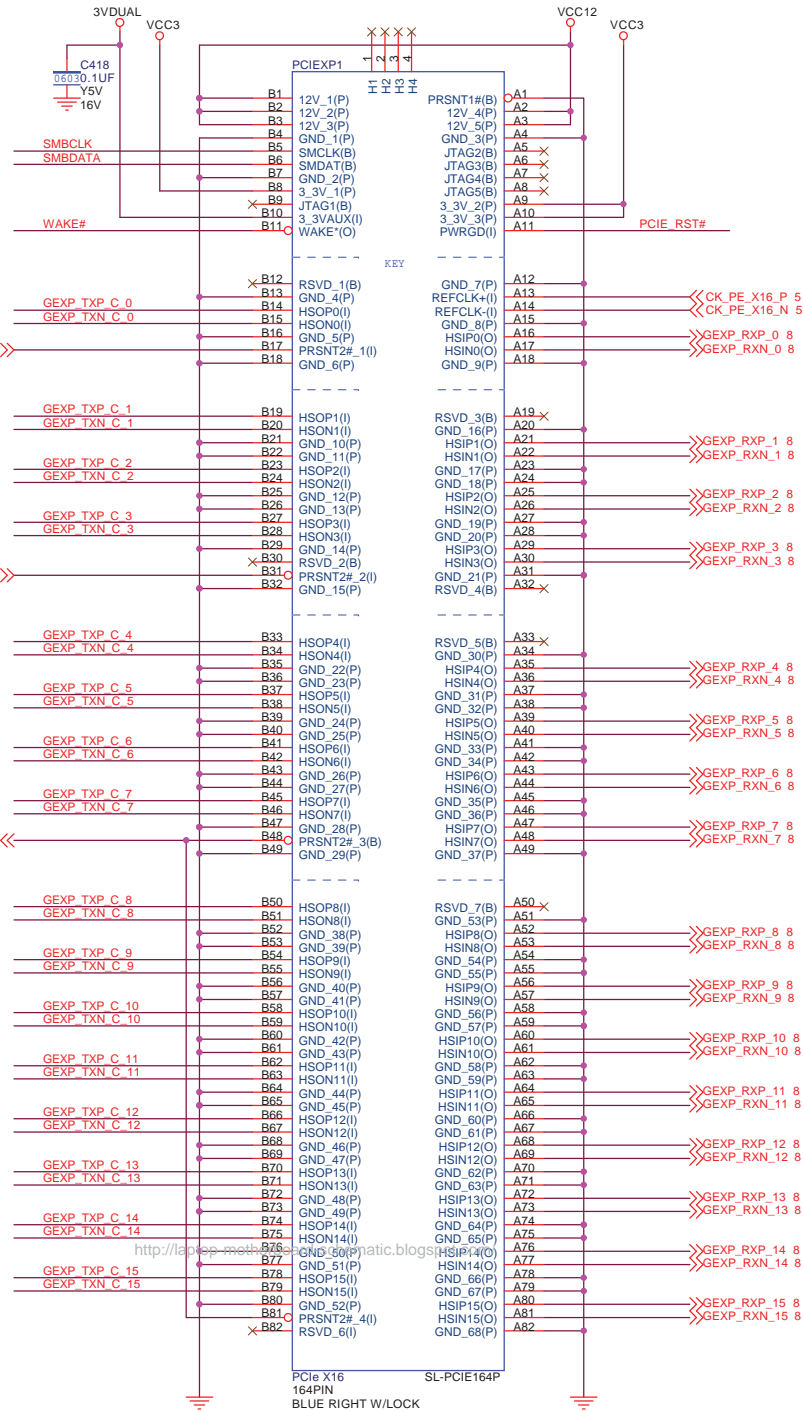
Channel B Address/Control switching Caps

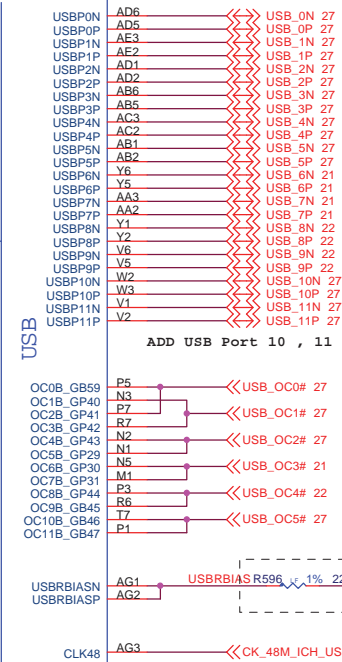
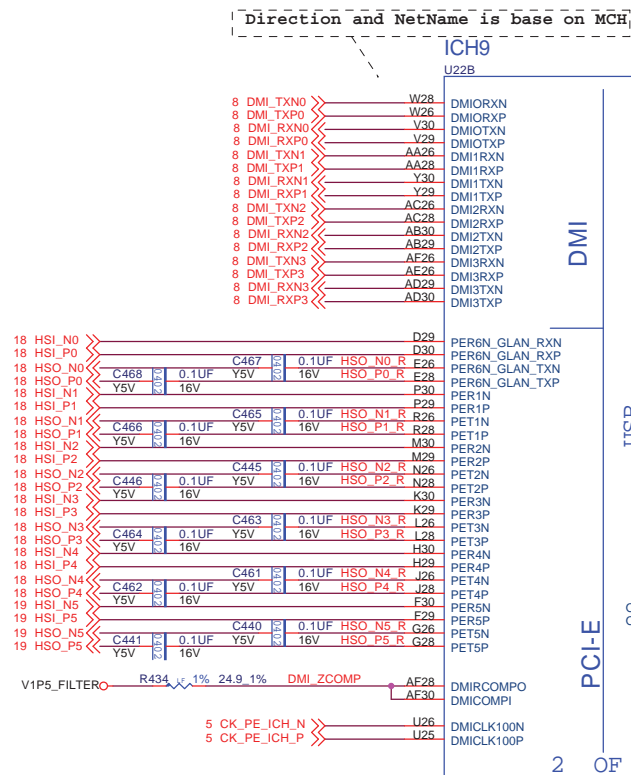
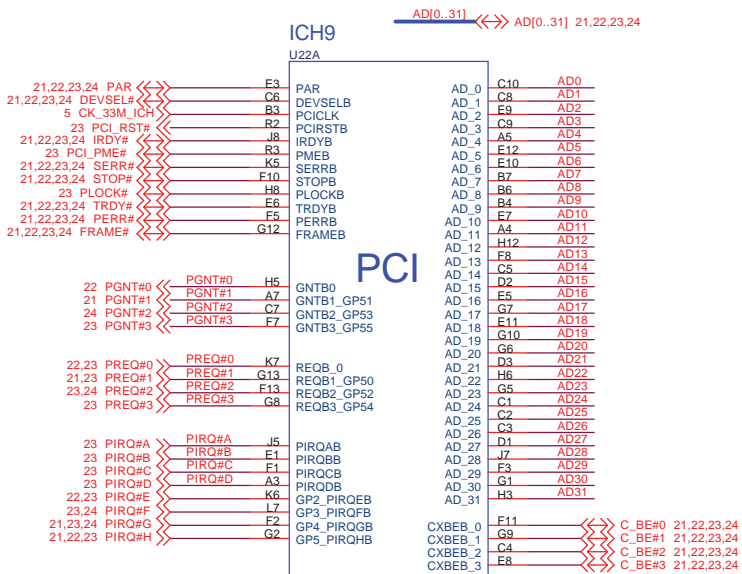


place at left and right ends of VTT island

<http://laptop-motherboard-schematic.blogspot.com/>

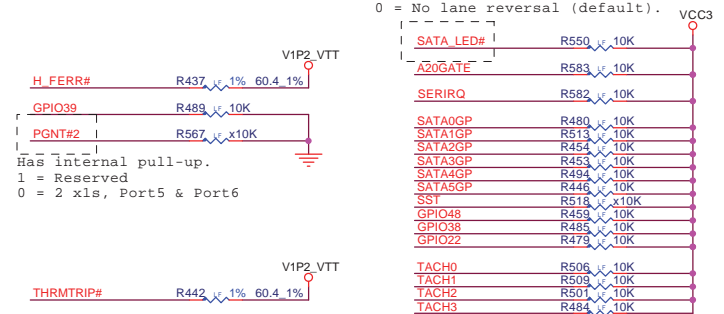
8 GEXP_RXP_0.7 << GEXP_RXP [0.7]
8 GEXP_RXN_0.7 << GEXP_RXN [0.7]
8 GEXP_RXP_8.15 << GEXP_RXP [8.15]
8 GEXP_RXN_8.15 << GEXP_RXN [8.15]
8 GEXP_TXP_0 >> C364 0.1UF GEXP_TXP_C_0
8 GEXP_TXN_0 >> C363 0.1UF GEXP_TXN_C_0
8 GEXP_TXP_1 >> C365 0.1UF GEXP_TXP_C_1
8 GEXP_TXN_1 >> C366 0.1UF GEXP_TXN_C_1
8 GEXP_TXP_2 >> C367 0.1UF GEXP_TXP_C_2
8 GEXP_TXN_2 >> C368 0.1UF GEXP_TXN_C_2
8 GEXP_TXP_3 >> C369 0.1UF GEXP_TXP_C_3
8 GEXP_TXN_3 >> C370 0.1UF GEXP_TXN_C_3
8 GEXP_TXP_4 >> C371 0.1UF GEXP_TXP_C_4
8 GEXP_TXN_4 >> C372 0.1UF GEXP_TXN_C_4
8 GEXP_TXP_5 >> C374 0.1UF GEXP_TXP_C_5
8 GEXP_TXN_5 >> C373 0.1UF GEXP_TXN_C_5
8 GEXP_TXP_6 >> C376 0.1UF GEXP_TXP_C_6
8 GEXP_TXN_6 >> C375 0.1UF GEXP_TXN_C_6
8 GEXP_TXP_7 >> C378 0.1UF GEXP_TXP_C_7
8 GEXP_TXN_7 >> C377 0.1UF GEXP_TXN_C_7
8 GEXP_TXP_8 >> C379 0.1UF GEXP_TXP_C_8
8 GEXP_TXN_8 >> C380 0.1UF GEXP_TXN_C_8
8 GEXP_TXP_9 >> C381 0.1UF GEXP_TXP_C_9
8 GEXP_TXN_9 >> C382 0.1UF GEXP_TXN_C_9
8 GEXP_TXP_10 >> C384 0.1UF GEXP_TXP_C_10
8 GEXP_TXN_10 >> C383 0.1UF GEXP_TXN_C_10
8 GEXP_TXP_11 >> C386 0.1UF GEXP_TXP_C_11
8 GEXP_TXN_11 >> C385 0.1UF GEXP_TXN_C_11
8 GEXP_TXP_12 >> C388 0.1UF GEXP_TXP_C_12
8 GEXP_TXN_12 >> C387 0.1UF GEXP_TXN_C_12
8 GEXP_TXP_13 >> C390 0.1UF GEXP_TXP_C_13
8 GEXP_TXN_13 >> C389 0.1UF GEXP_TXN_C_13
8 GEXP_TXP_14 >> C392 0.1UF GEXP_TXP_C_14
8 GEXP_TXN_14 >> C391 0.1UF GEXP_TXN_C_14
8 GEXP_TXP_15 >> C394 0.1UF GEXP_TXP_C_15
8 GEXP_TXN_15 >> C393 0.1UF GEXP_TXN_C_15



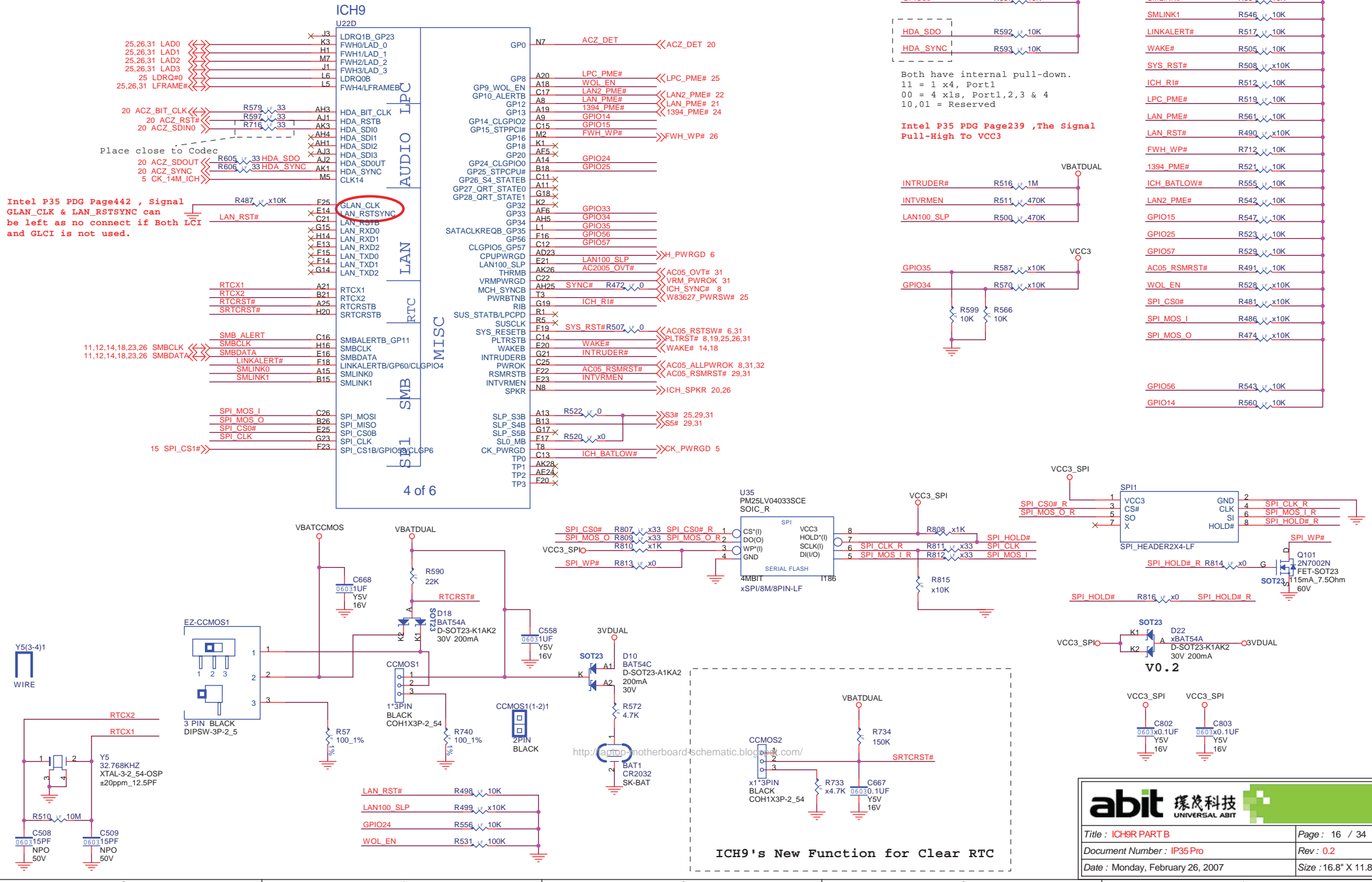


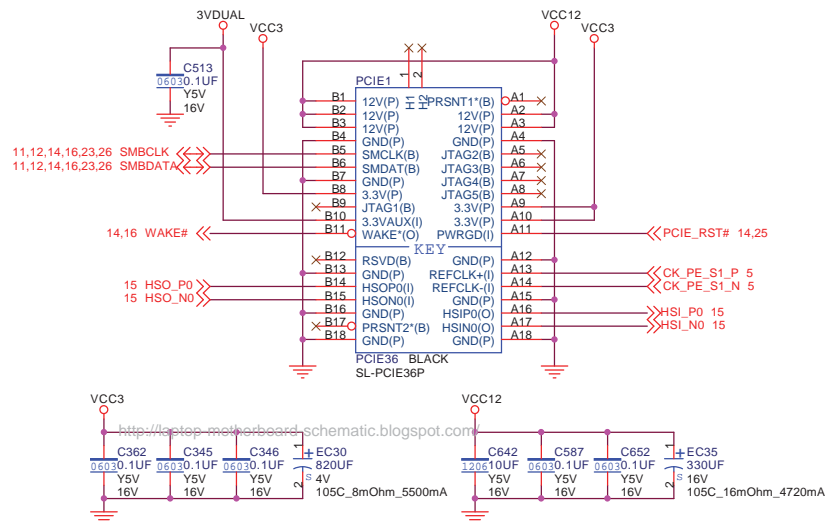
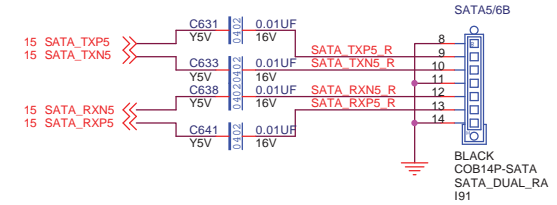
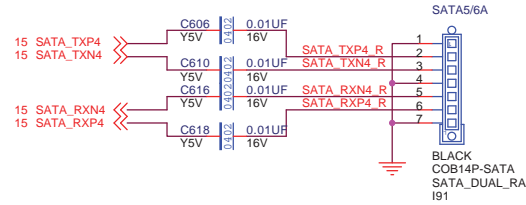
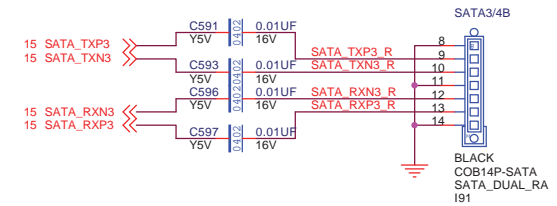
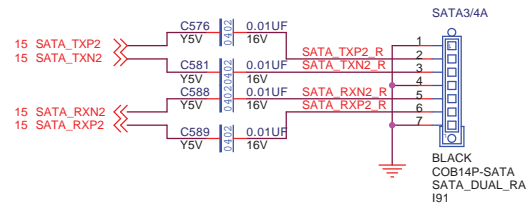
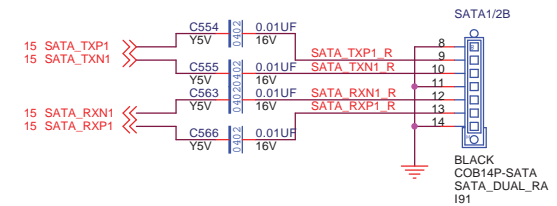
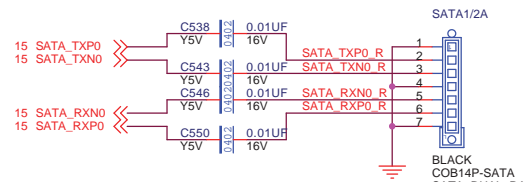
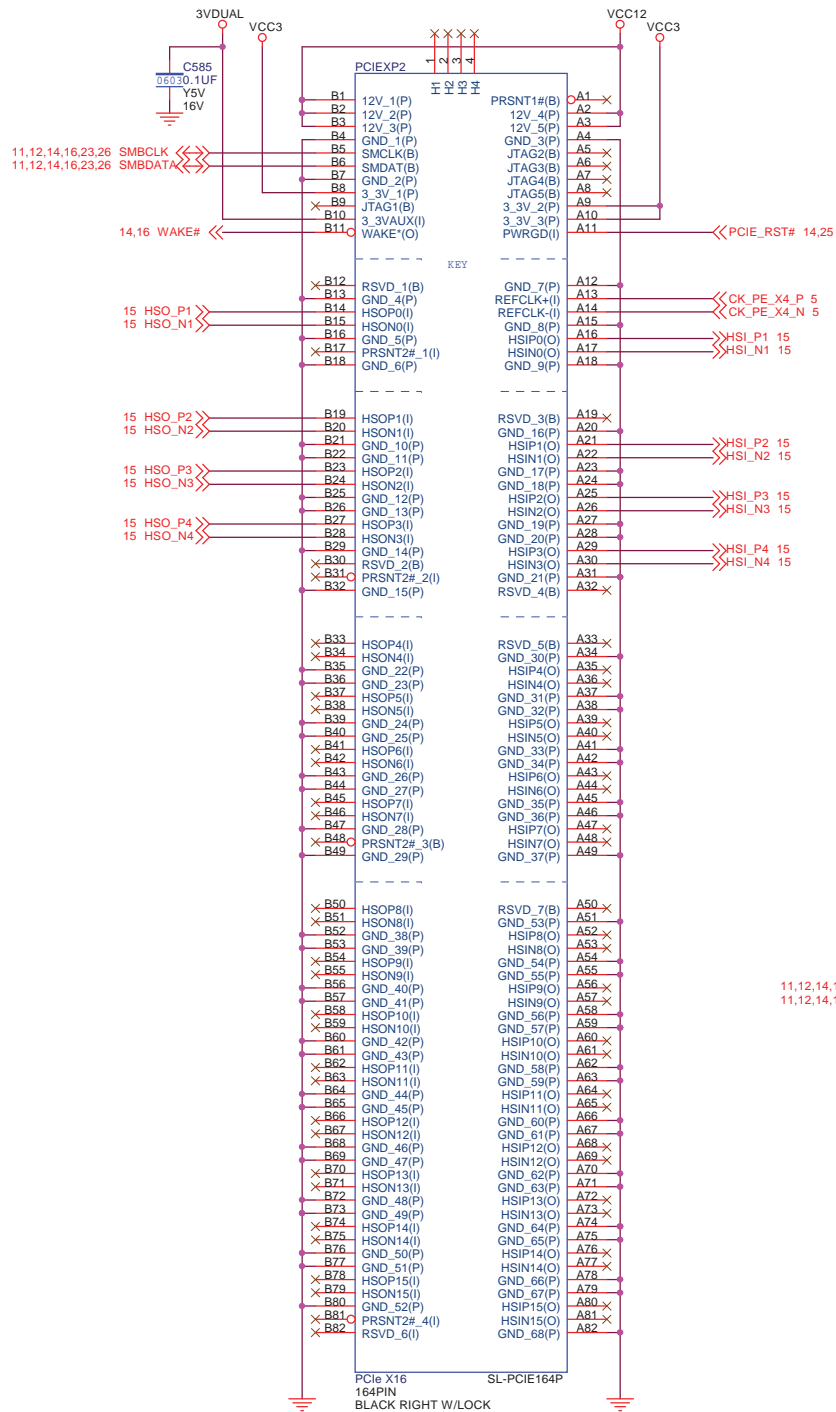
GNT0#	SPI_CS1#	Boot BIOS Destination Selection
0	0	Reserved
0	1	SPI
1	0	PCI
1	1	LPC

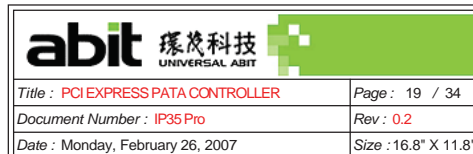
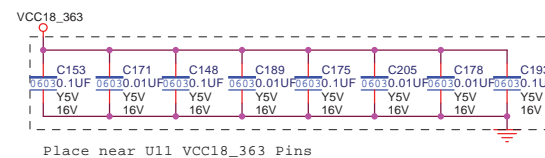
Has internal pull-up.
1 = Lane 0-3 are reversed.
0 = No lane reversal (default).

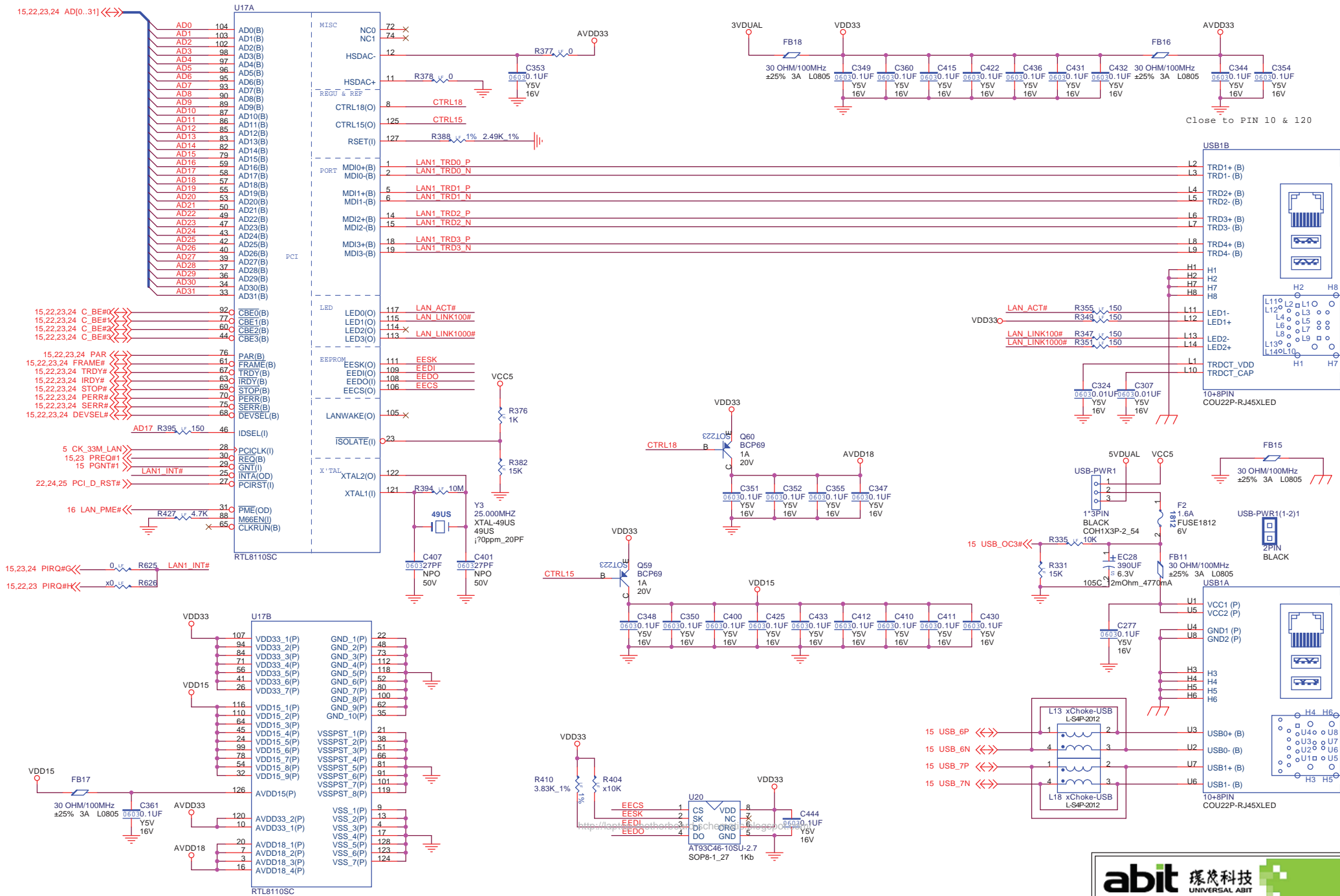


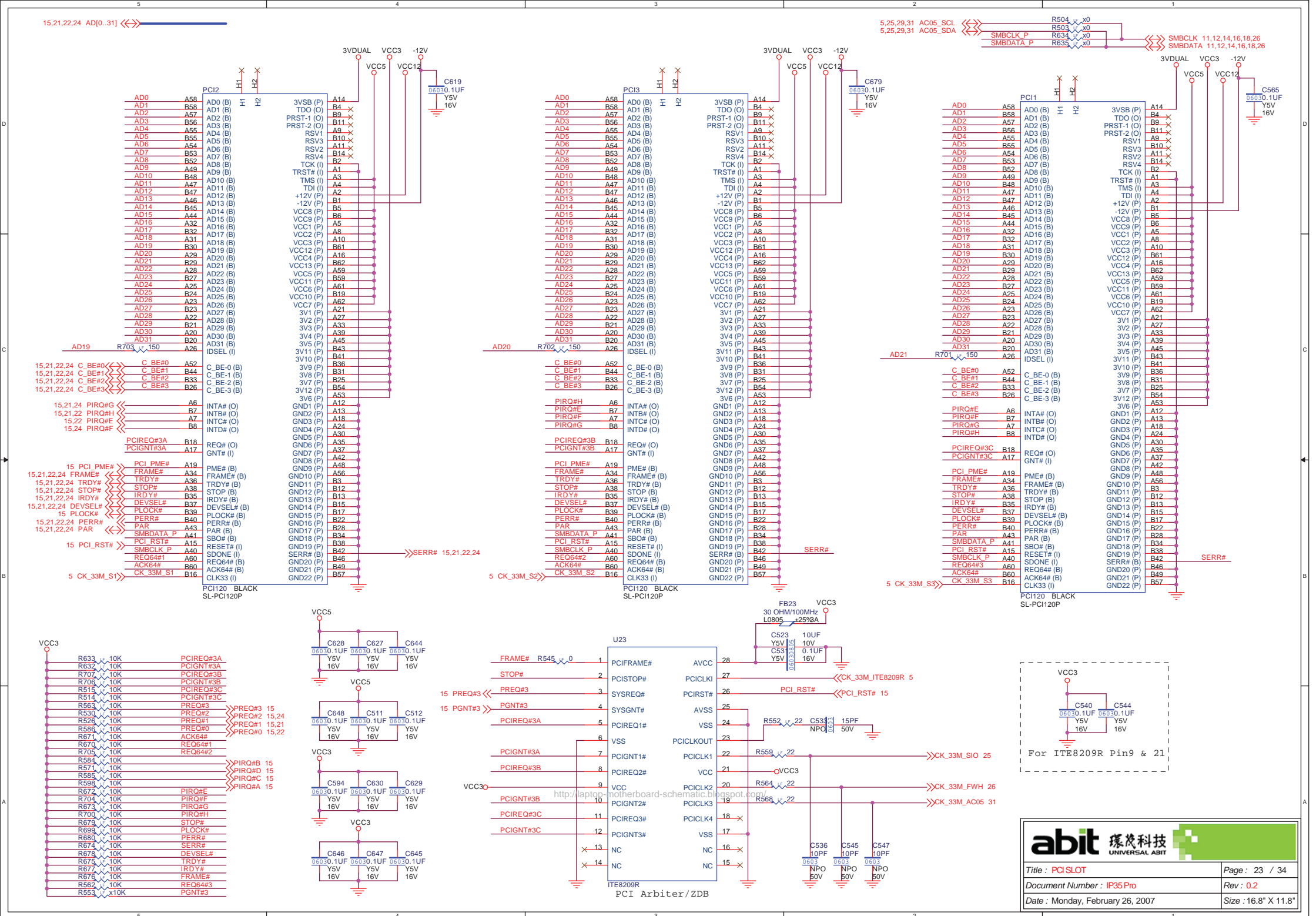
Model	GPIO34	GPIO35
xxx	0	0

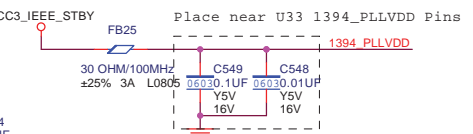
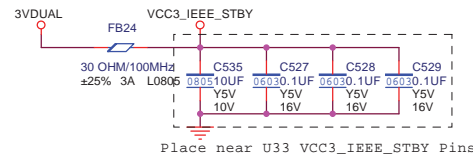
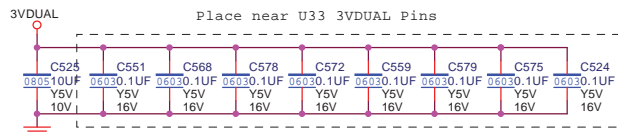




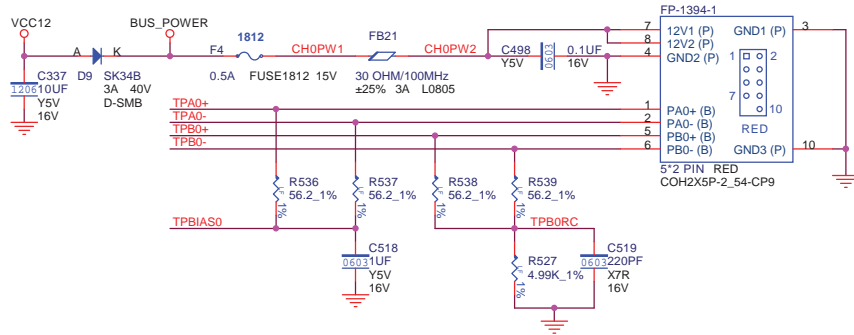




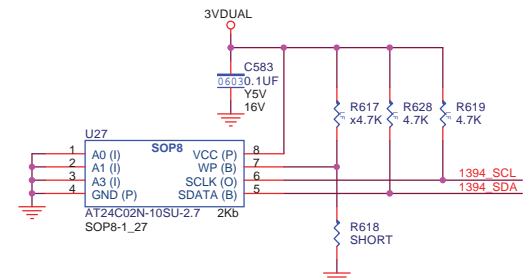
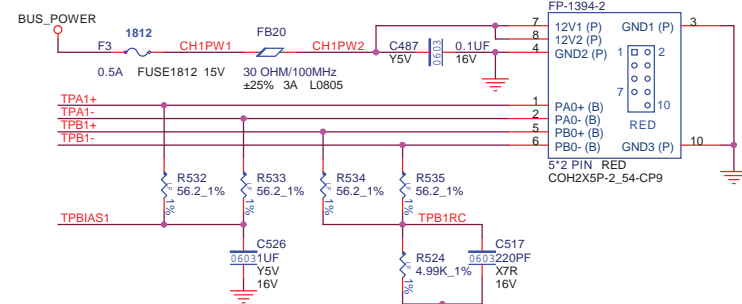




IEEE-1394 Channel 1



IEEE-1394 Channel 2



TSB43AB22

PCI BUS INTERFACE

PHY PORT 2

BIAS CURRENT

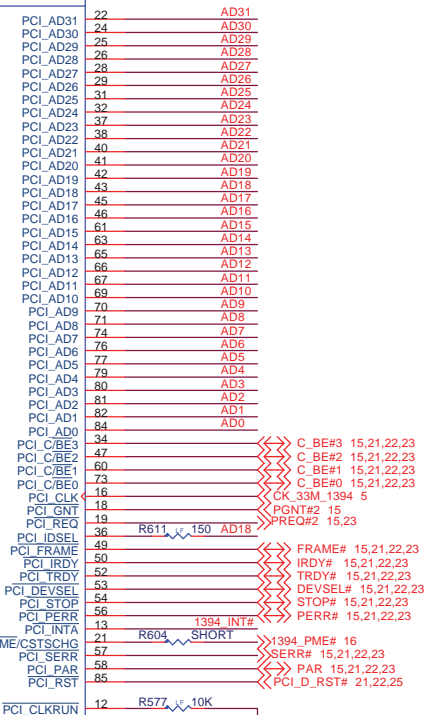
OSCILLATOR

FILTER

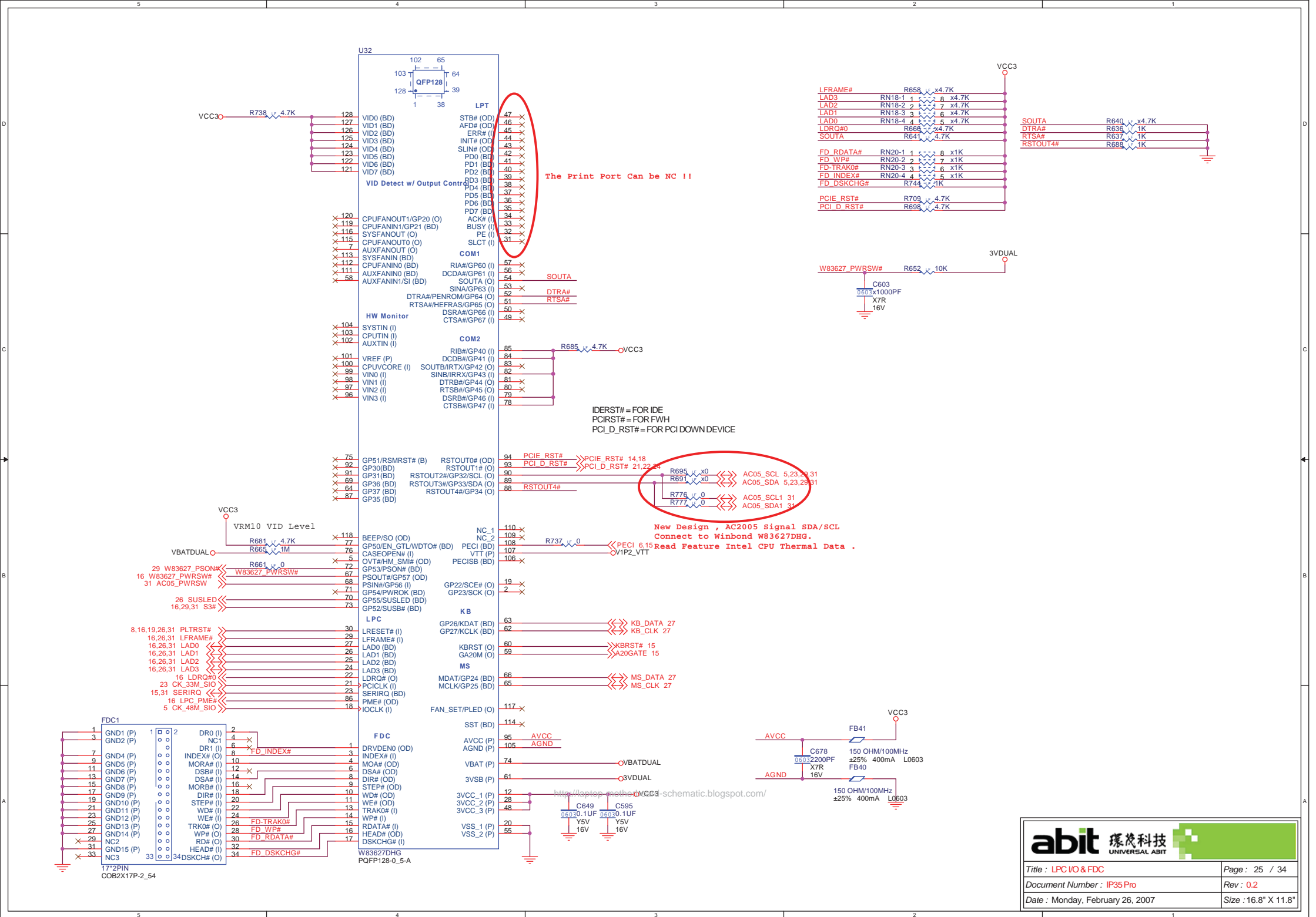
EEPROM 2 WIRE BUS

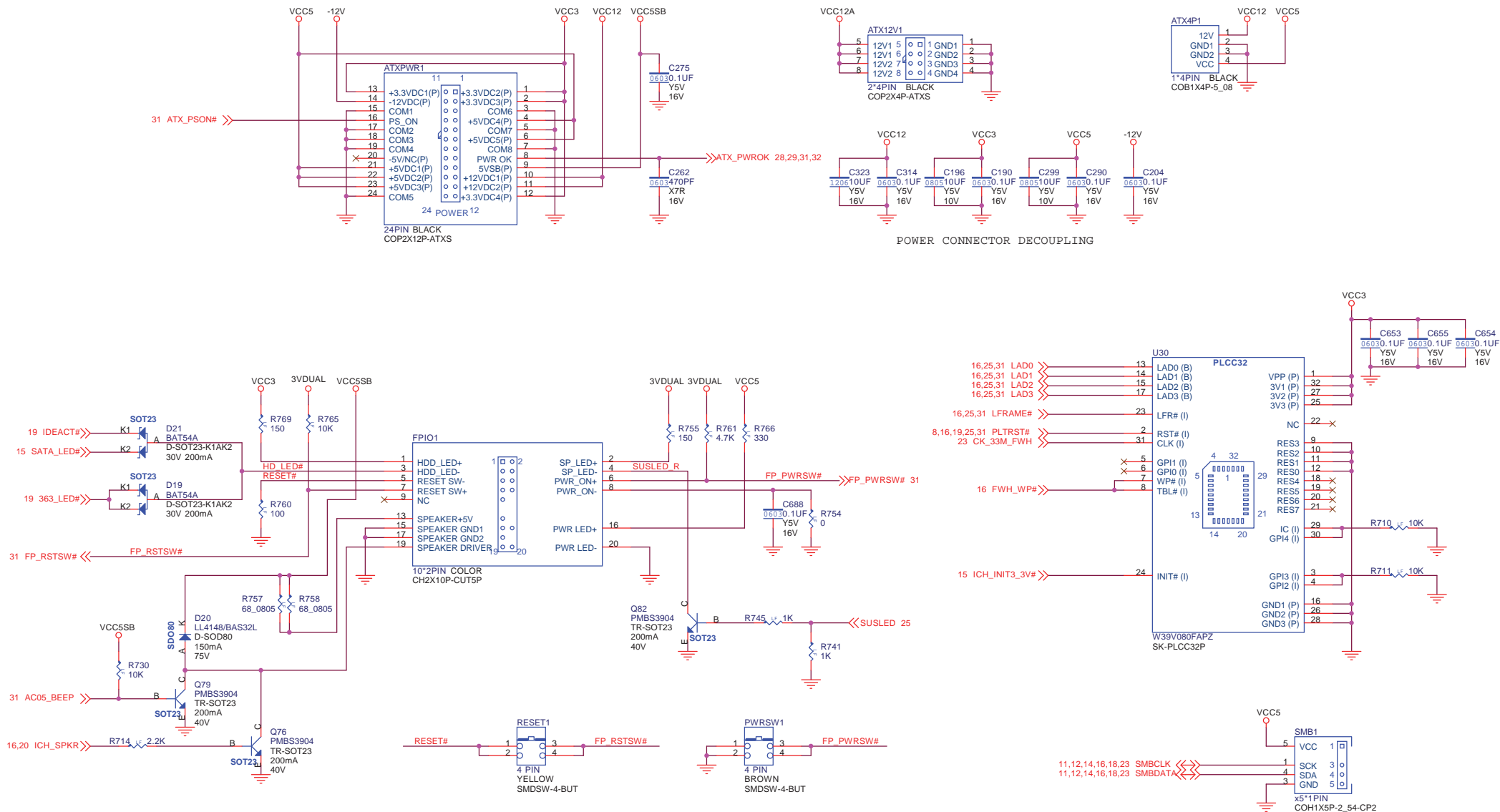
POWER CLASS

PHY PORT 1



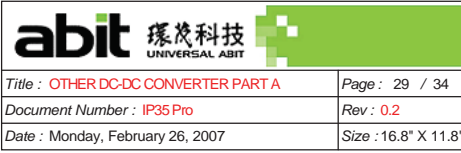
<http://laptop-motherboard-schematic.blogspot.com/>

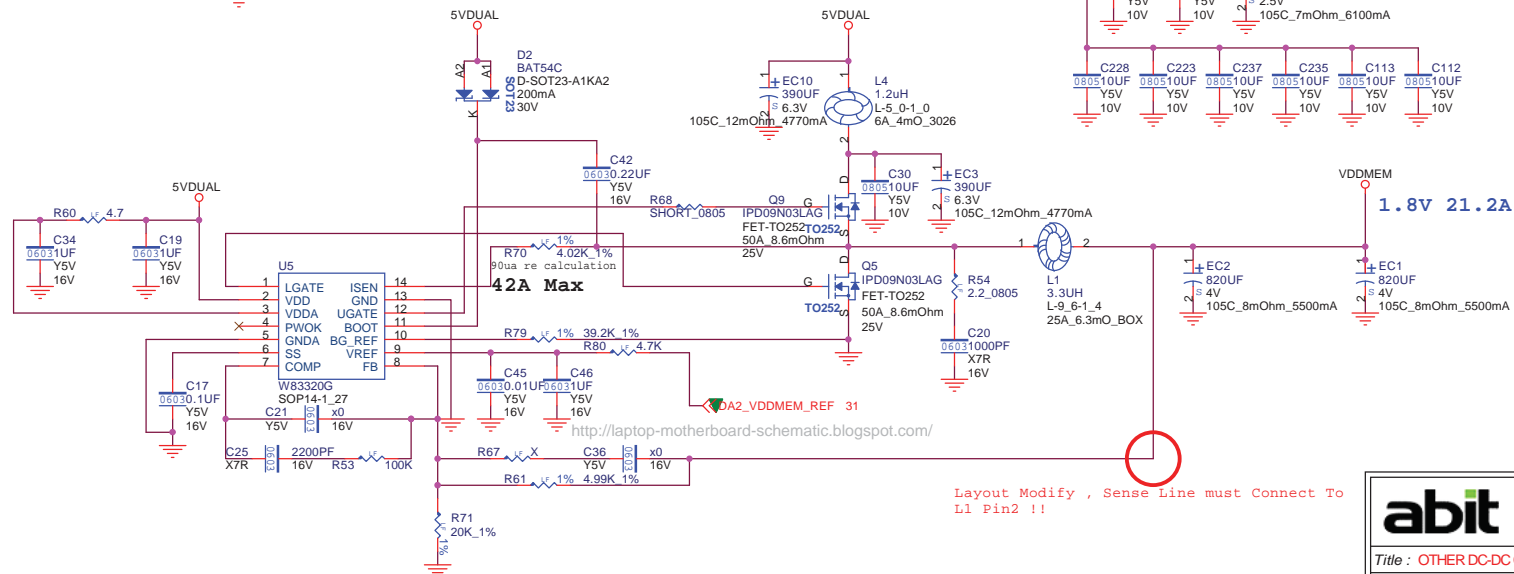
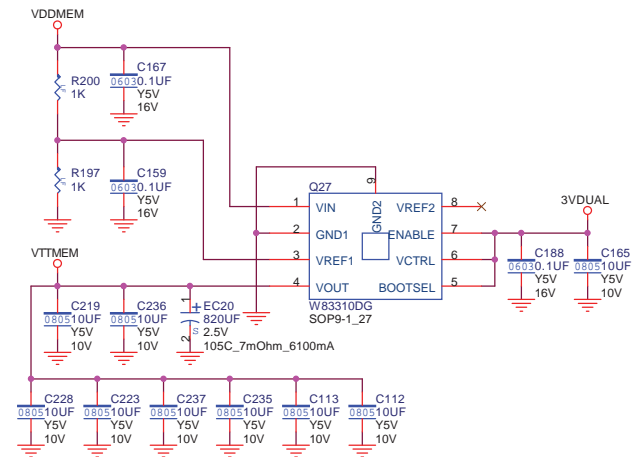
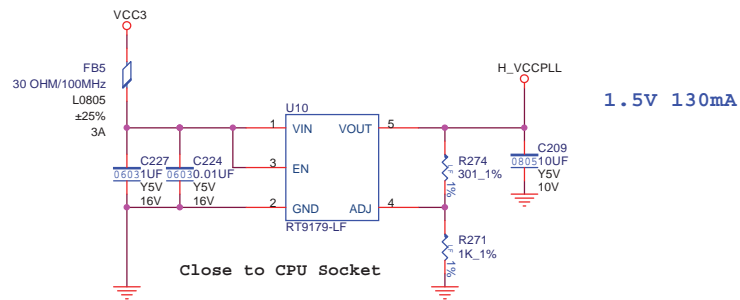
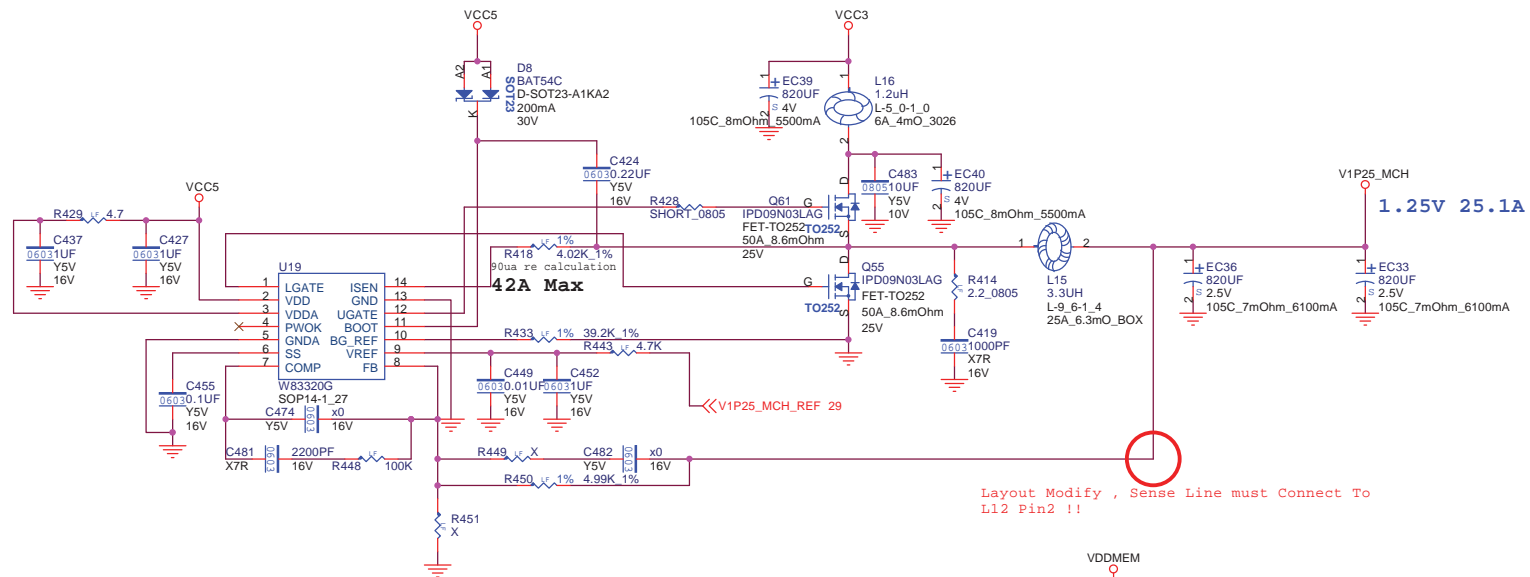


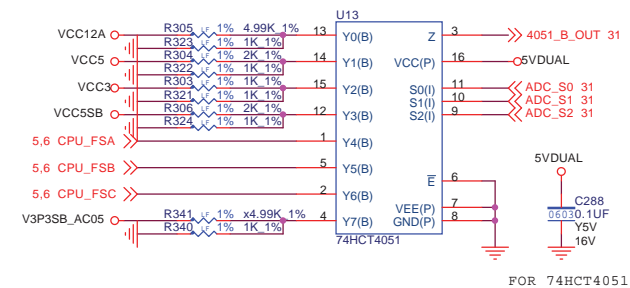
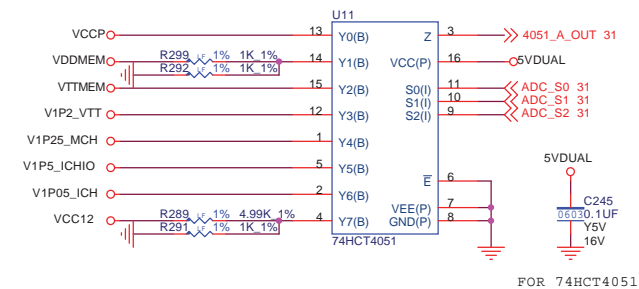
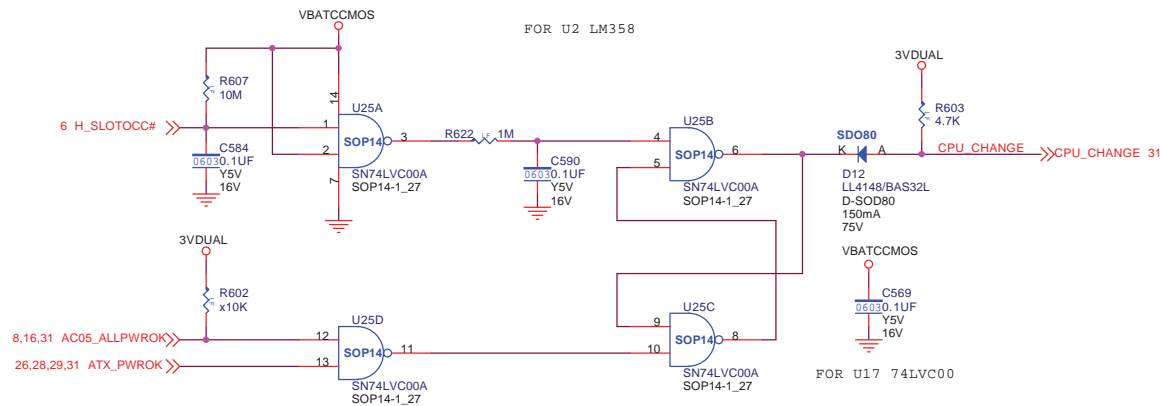
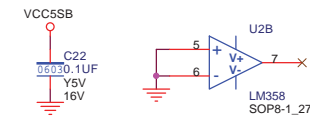
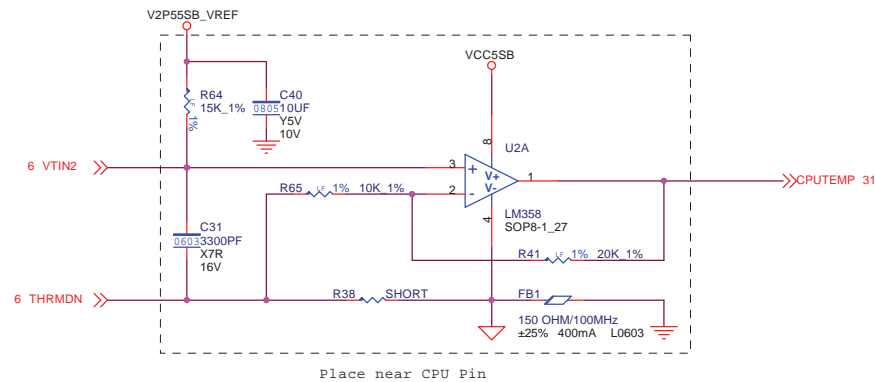


<http://laptop-motherboard-schematic.blogspot.com/>



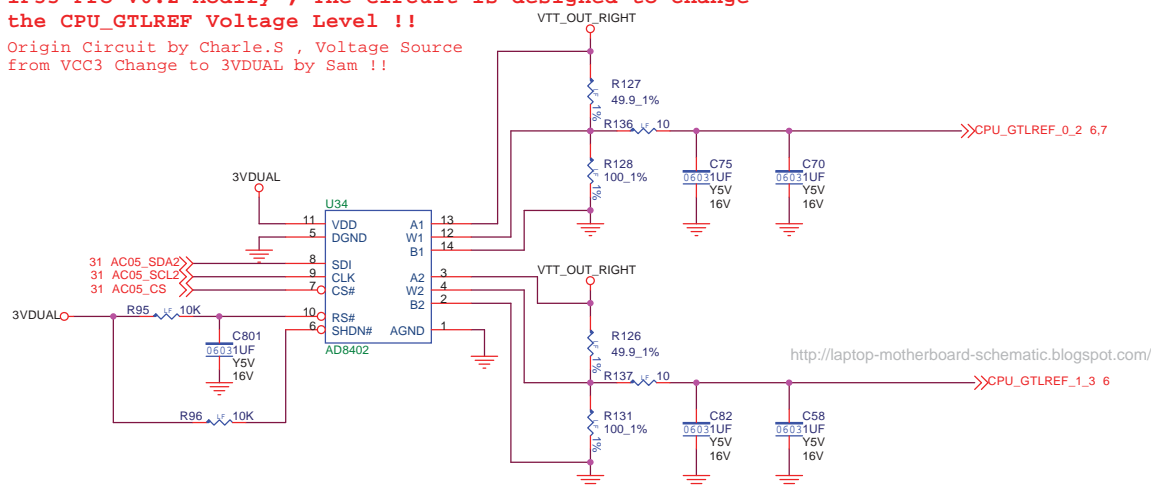


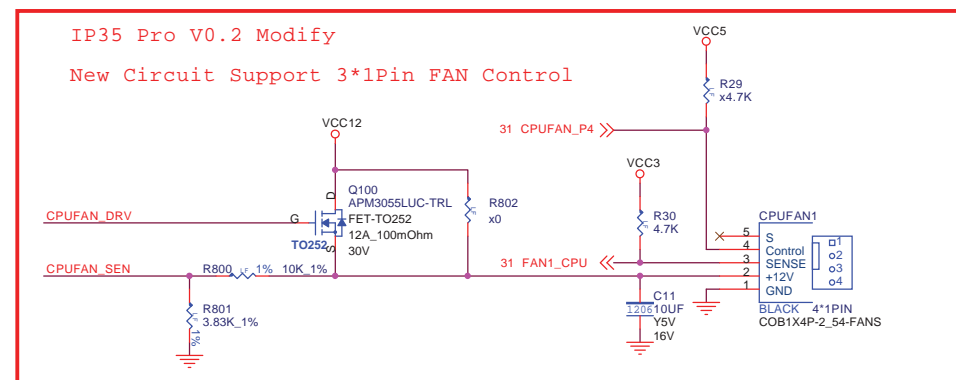
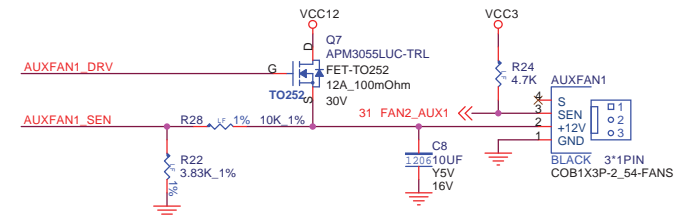
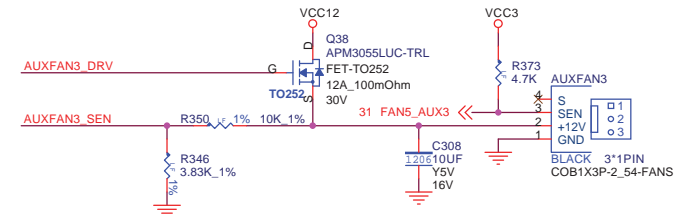
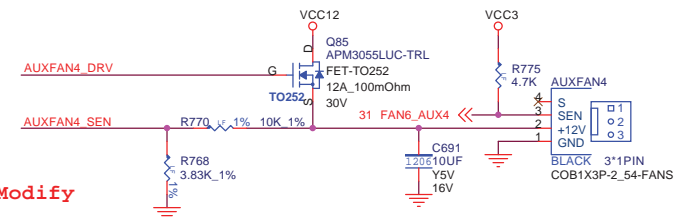
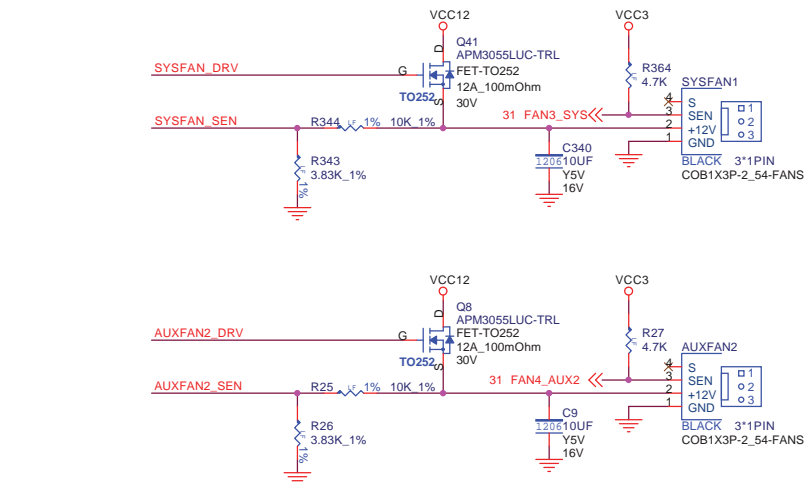
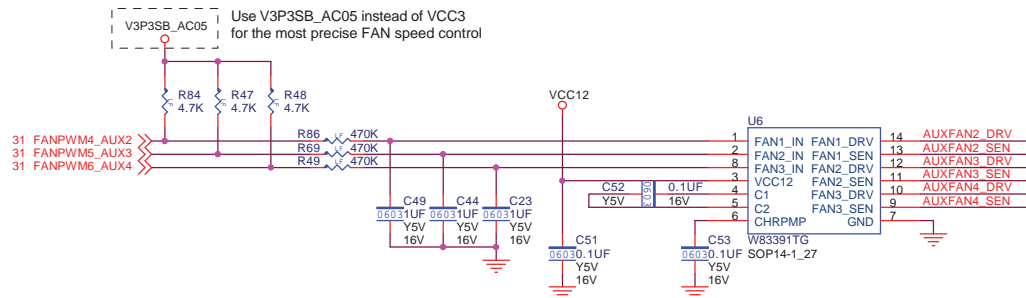
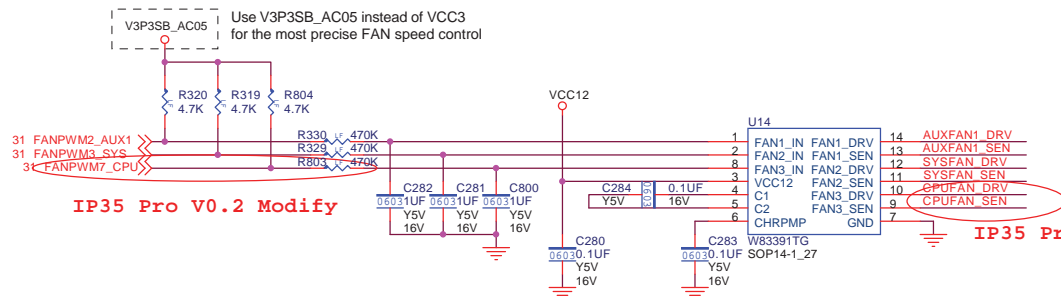




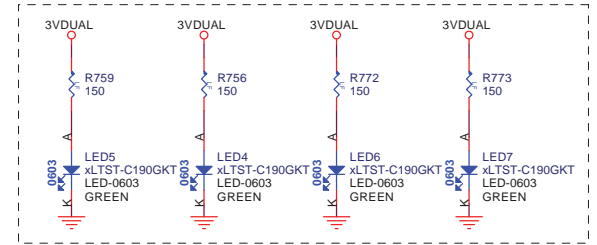
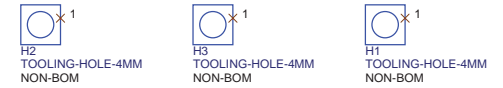
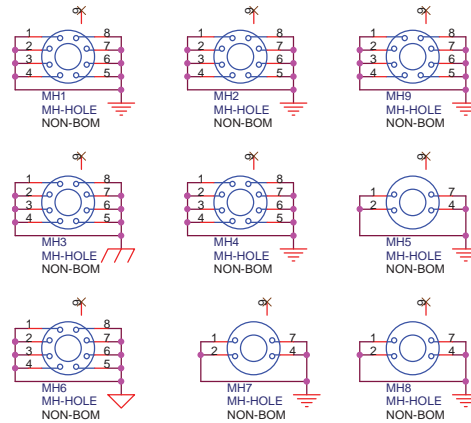
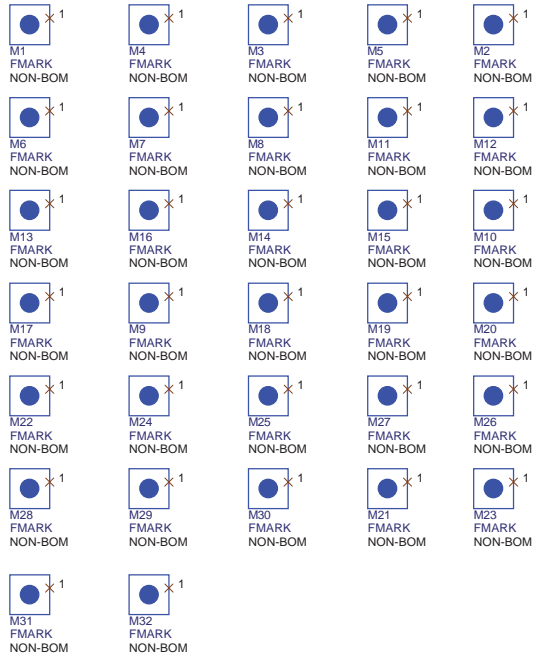
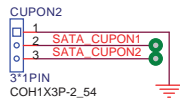
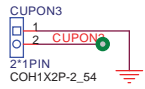
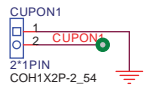
IP35 Pro V0.2 Modify , The Circuit is designed to change the CPU_GTLREF Voltage Level !!

Origin Circuit by Charle.S , Voltage Source from VCC3 Change to 3VDUAL by Sam !!

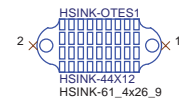
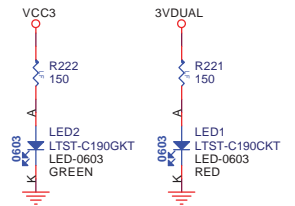
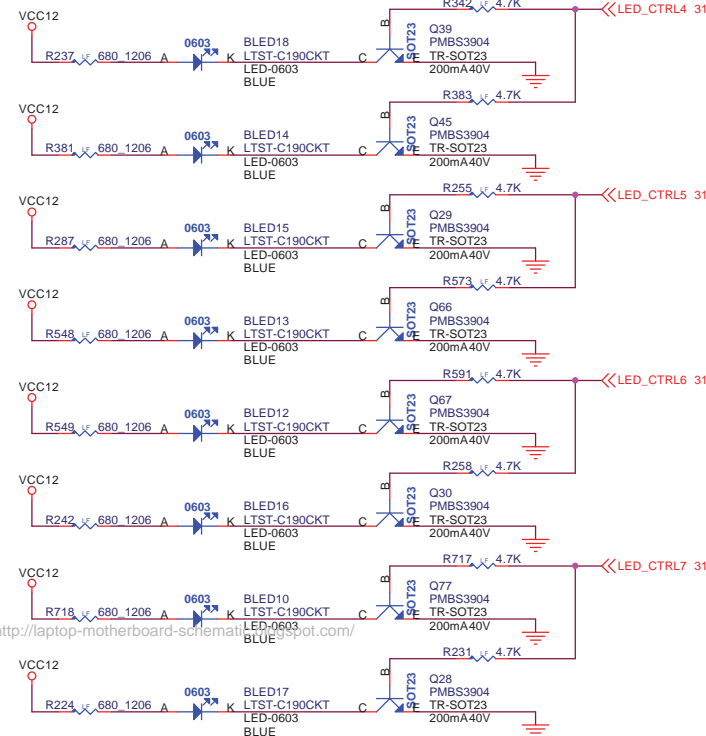
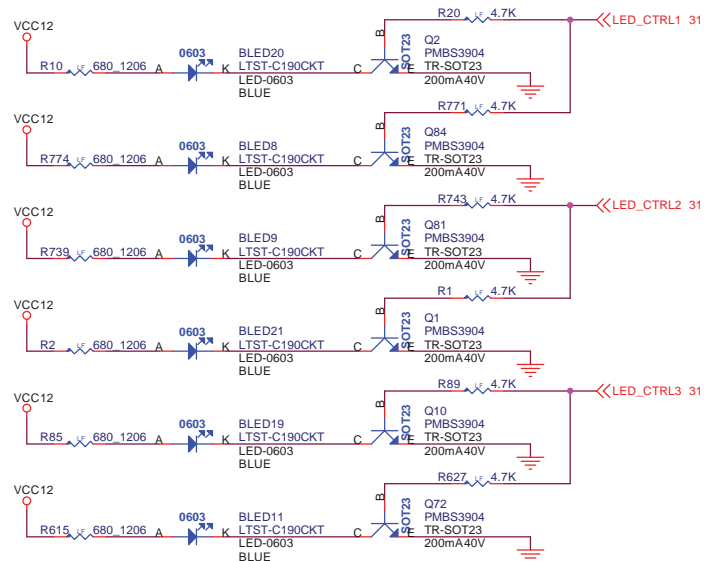




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Place close to FPIO1



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